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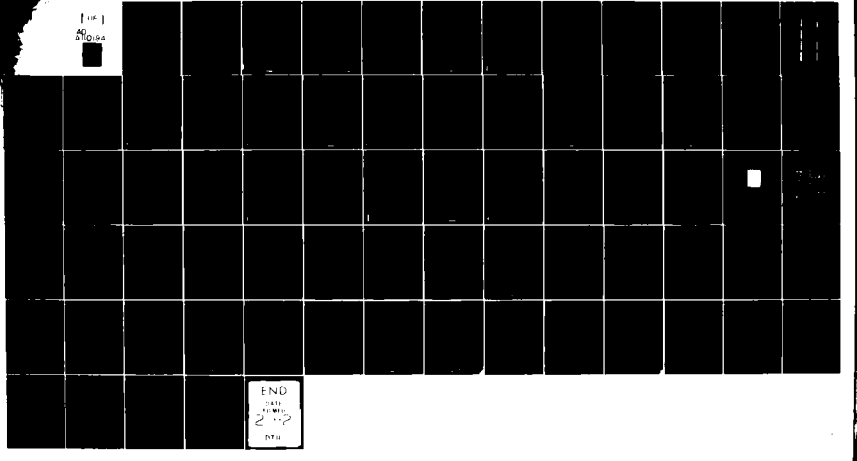

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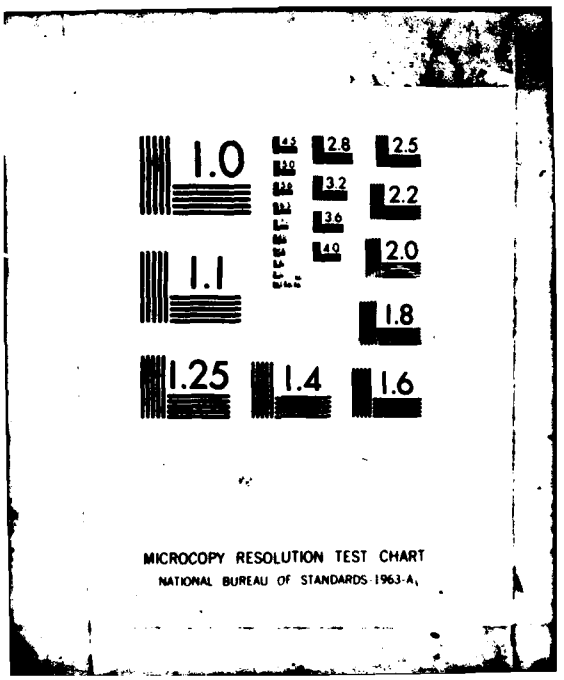
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SOS ELECTRICAL OVERSTRESS INVESTIGATIONS

Rockwell International Corporation
P.O. Box 3105
Anaheim, California 92803

31 March 1978

Final Report for Period 1 April 1977—31 March 1978

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20 ABSTRACT (Continue on reverse side if necessary and identify by block number)

The SOS Electrical Overstress Investigations program was initiated to isolate the mechanisms of second breakdown. Tests conducted at Auburn University identified the need for test diodes with specified inherent silicon properties and controlled sets of processed "defects". Rockwell International designed and fabricated two wafer lots of SOS p-n diodes with a wide range of physical design variations and process parameter variations to fulfill the need for special test diodes. Design requirements traversed the limits of the state-of-the-art in processing capabilities, but all of the design goals were realized in the final wafer

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20. ABSTRACT (Continued)

product. "Defects" as small as one micron were faithfully produced on both wafer lots. Each die on the wafer contains 214 diodes and there are five different substrate doping levels (five different wafers) to yield 1070 diode variations in a wafer lot. The need expressed by Auburn University for special diodes has been fulfilled.

SUMMARY

The study of secondary breakdown of silicon-on-sapphire (SOS) diodes by physicists at Auburn University identified the need for special device structures to determine the precise mechanisms of second breakdown. Rockwell International provided the expertise for design and fabrication of SOS p-n diodes with a full range of process parameter variations and physical design variations. Two lots of the special SOS diodes have been fabricated, electrically characterized, and delivered to Auburn University. An indication of the design diversity and quantity of SOS test diodes involved is given in the following summary.

- Standard reference structures — 25 devices
- Contact/diffusion spike structures — 80 devices
- Enclosed reference structures — 20 devices
- Half-size spike structures — 20 devices
- Multiple spike structures — 51 devices
- Four-terminal structures — 6 devices
- Doping level test structure — 1 devices
- Interdigitated structures — 2 devices
- Radius of curvature structures — 9 devices

214 devices per die

- 70 dice/wafer (some edge loss) = 14,980 devices/wafer
- No. devices/lot = 214 x 70 x 5 wafers/lot = 74,900
- No. design variations/lot = 214 x 5 = 1070
  (Five starting material doping levels)

Based upon the second-breakdown test requirements for the Auburn University study, the design and fabrication goals of the SOS Electrical Overstress Investigations program have been achieved.

Device design was oriented toward determining structural impact on the initiation of second breakdown and the resulting filamentation melt paths. To identify specific mechanisms and synergisms, it is recommended that a failure analysis effort be conducted in support of Auburn University's second-breakdown tests. Also, the second breakdown tests progress, new design (and analysis) requirements will evolve. To satisfy these requirements, it is recommended that additional wafer-lots of SOS diodes be fabricated to address the new design, test and analysis data.

PREFACE

The SOS Electrical Overstress Investigations program is sponsored by the Defense Nuclear Agency under RDT&E RMSS Code B323077464 Z99QAXTB09703 H2590D. The purpose of the program is to determine the specific mechanisms of secondary breakdown and to provide a mathematical model to describe this phenomenon. Rockwell International is contributing to this goal by providing SOS p-n diodes with a wide range of design and process variations aimed at isolating these mechanisms.

Acknowledgements are due to many contributors to this phase of the program. Dr. D. Howard Phillips, a Rockwell co-principal investigator, was instrumental in coordinating preliminary activities between Rockwell International, DNA (MIRADCOM), Braddock-Dunn-McDonald, Mississippi State University, Purdue University, University of Alabama, and Auburn University. Dr. David Mathews of DNA (MIRADCOM), technical monitor, Mr. David Alexander of BDM, and Dr. D. Wunsch of USAF/AFWL performed much of the preliminary groundwork. At Rockwell International, Mr. M. D. Barry and Mr. J. L. Peel provided the processing expertise. Mr. B. Peterson and Mr. T. R. Day performed the mask layouts. Mrs. M. E. Glowna assisted with electrical characterization. Ms. B. Vandra, Ms. J. Landers and Ms. C. Wallace contributed significantly to the preparation of this report.

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1. INTRODUCTION

1.1 PROBLEM STATEMENT

Silicon-on-Sapphire (SOS) p-n diodes have not been fabricated with a full range of process parameter variations and physical design variations aimed at isolating the precise mechanisms of second breakdown. One of the major problems in second breakdown studies of SOS devices is a lack of critical parameter variations in existing test structures. Results have been obtained which point out the need for more definition. For example, hotspot location versus inhomogeneities in the junction diffusion has been noted, although not firmly related, by Dr. Paul Budenstein and co-workers at Auburn University. Fabrication of special SOS p-n junction test devices is necessary to finalize the conclusions drawn in the work of Dr. Budenstein, et al.

1.2 BACKGROUND

1.2.1 SOS Junction Breakdown

Secondary breakdown of SOS diodes has been studied and described (Ref 1) by physicists at Auburn University. The application of an electrical pulse (pulse-power electrical overstress) was used to induce secondary breakdown. The information in this section is a summary of information reported in Reference 1. Second breakdown is a descriptive term that covers a range of current filament phenomena in junction systems. Phenomenologically, it is a transition to a high conductance state that occurs at high current densities. If the external circuit constrains the total current in the device to a constant value, then the transition is accompanied by a voltage drop. The current and temperature distributions in the system change dynamically during the filamentation process; these changes cannot be modeled as a succession of steady-state conditions. For many years it was not possible to define the basic mechanisms associated with second breakdown, although numerous plausible suggestions were made and each contained merits. The breakthrough for delineating the correct mechanisms came with the work of Sunshine and Lampert (Refs 2 - 5). The studies of Budenstein, et al (Refs 6 - 9) followed, using the stroboscopic method developed by Sunshine. The stroboscopic method allows instantaneous current distributions to be observed in transparent thin-film silicon devices because the transmissivity is a strong function of the film temperature. From studies of silicon-on-sapphire thin-film diodes, the following description of second breakdown has emerged (Refs 2 - 9). The features of this description are consistent with the phenomena reported for three-dimensional systems of many different geometries and, hence, are truly descriptive of second breakdown.

The number of junction channels that form prior to filament growth depends on the pulse length--i.e., as pulse length decreases, the number of channels increases. The current amplitude for junction channel formation increases as pulse width decreases. Since the location of the channels is different for pulses of different length, it seems that inhomogeneities play only a secondary role in channel nucleation; the locations are determined primarily by the heat flow and electrical conduction equations.

In second-breakdown studies, the time from the leading edge of the exiting pulse to the beginning of the voltage drop is called the delay time. For non-destructive second breakdown, the voltage drop starts after all filaments have nucleated. For the destructive form, the voltage drop occurs when the melt starts to grow. The times of occurrence are different; however, if the amplitude of the exciting pulse is increased far above threshold, then the two resulting voltage drops appear to occur almost similtaneously. Filament growth involves heating of the lightly doped region. At the threshold for melt formation, the portion of the lightly doped region of silicon that is not part of the filament is at a temperature close to that of the peak of the temperature-resistivity curve. Thus, the delay time for destructive second breakdown is associated with the heating of the lightly doped region. The thermal time constants are approximately 5 - 10 μsec. A power-time relationship suggested by Flemming (Ref 10) is

$$p\tau_d^n \sim \text{constant}$$

The exponent, n, in this equation has been observed to range from 0.17 to 1.0 for various types of p-n junctions.

Hence, in the description of second breakdown, the delay time to the onset of destructive breakdown is related to the temperature of the lightly doped region. When this temperature reaches a value corresponding to the peak of the temperature-resistivity curve, a filament bridges the lightly doped region and a melt channel forms. At high power levels, consistent with the results of Ferry and Dougal (Ref 11), the product $p\tau_d$ seems to approach a constant value.

Since the events of SOS junction second breakdown are not well established with respect to device parameters, completely descriptive models do not yet exist. Questions remain regarding the roles of thermal and electronic effects in SOS diode second breakdown.

Semiconductor junction second breakdown has been studied by many investigators. Several diverse measurement and observation techniques have been employed. SOS diodes have added another dimension to these studies because of the ability to transmit visible light through the transparent sapphire substrate. Further, since the optical transmittance is an inverse function of temperature, it can be used to locate hotspot areas created as second breakdown levels are reached. Investigators in this area have used stroboscopic observations of electrically pulsed junctions to obtain a photographic time history of the current distribution during a single pulse (Ref 2 - 3). As these tests have progressed, the need has developed for refinements in test procedures, photographic methods and in the SOS test devices.

2. TECHNICAL APPROACH

2.1 GENERAL

Rockwell International's approach to the problem was to design and fabricate special SOS diode test structures to support continuing electrical overstress work on second breakdown. These structures were designed for use in the stroboscopic experimental methods briefly described in the Appendix and more fully in Reference 12. Diodes used in these tests must be designed such that the junction is visible, i.e., not covered by metallization, so that current-density patterns such as those in Figure 1 can be observed. Definitive tests will be greatly enhanced by using diodes with controlled design and process variations to investigate the second breakdown mechanisms. The design variations planned for special SOS diode structures are described in the following section. The SOS Electrical Overstress Program Flow Diagram outlining the functional relationships is presented in Figure 2.

2.2 DEVICE DESIGN AND FABRICATION

Test devices designed and fabricated under this program include SOS p-n diodes and simulated bipolar devices for characterization and analysis by Auburn University. These devices were fabricated with a sufficiently large range of physical and processing parameters to permit the determination of electrical-overstress-induced junction second breakdown failure thresholds as related to (1) inherent silicon properties, (2) fabrication properties, and (3) quality control properties.

Device characteristics such as:

- Background doping concentration
- Effects related to junction radius of curvature
- Metallization defects
- Lateral diffusion spikes
- Diode body width
- N^+ to P^+ separation distance

have been considered for this purpose.

Devices fabricated for this program have utilized a proven, cost-effective, multi-cell mask design. The mask design contains multiple cells so that a number of special test devices are included in a single mask design. Each wafer contains all the test devices and demonstration vehicles required to meet the 2nd breakdown diode-characterization objective of this program. This approach is routinely employed in R&D programs requiring a variety of special test structures and demonstration vehicles. Hardened Complementary Metal-Oxide-Silicon/Silicon-on-Sapphire (CMOS/SOS) technology was employed to fabricate SOS transistors and SOS diodes with various design and processing parameters.

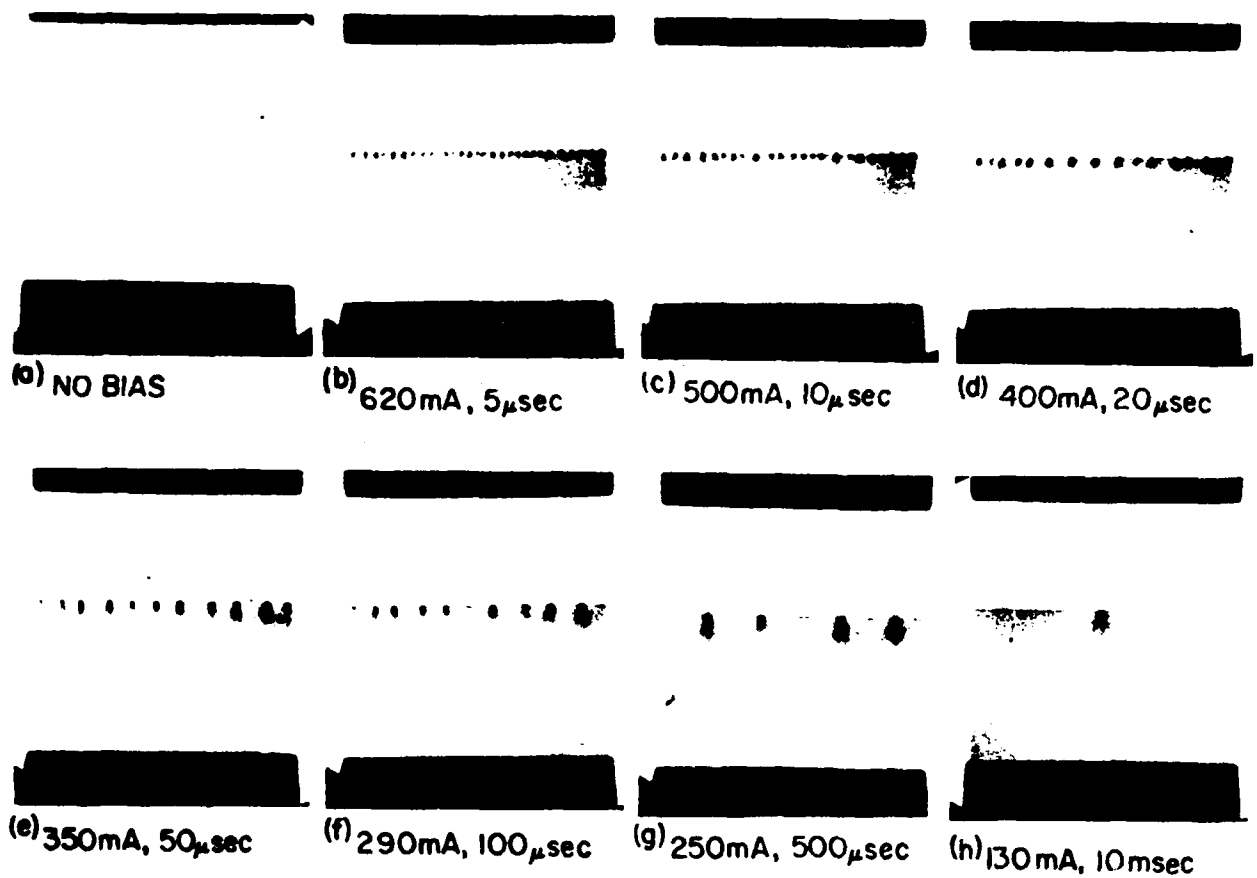


Figure 1. Optical transmission patterns taken with the strobe light at the end of the current pulse for a range of pulse lengths 5 μsec to 10 msec. The current amplitude in each case was adjusted to yield a maximum number of dark spots (Reference 7, Page 52). The SOS diode test devices for this program were designed to allow visual inspection of the p-n junctions during pulse-power electrical overstress tests.

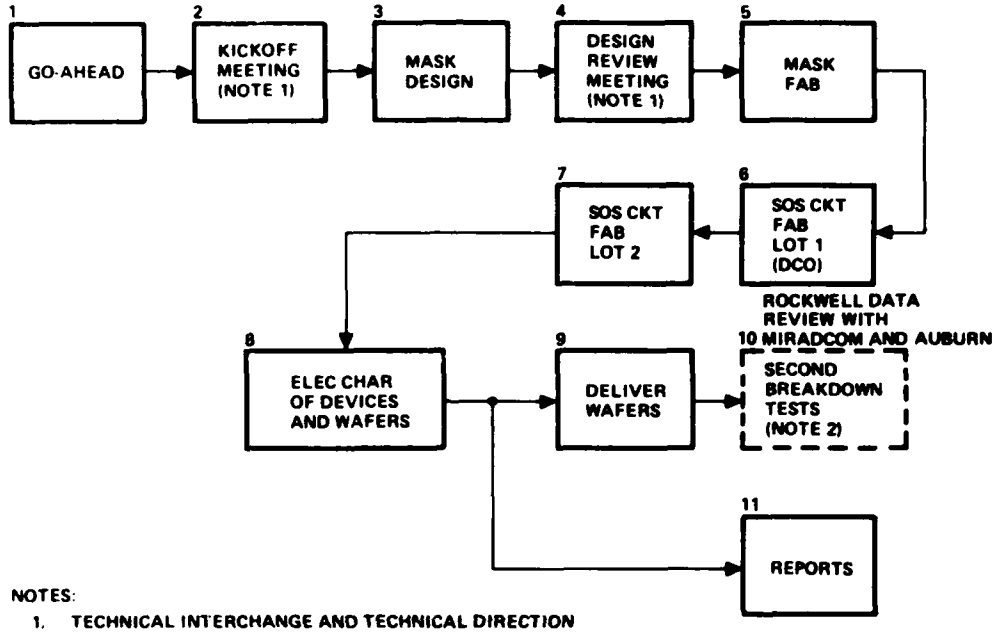


Figure 2. SOS Electrical Overstress Investigation Program Flow Diagram

2.3 MASK DESIGN AND GENERATION

For the SOS Electrical Overstress Investigation Program, the following steps were used in the development of the 13 required masks:

Step 1: Circuit design and analysis

Step 2: Circuit layout

Step 3: Digitization/MOS-DRAW

Step 4: Tape generation

Step 5: Pen-plot

Step 6: Color guides and mask generation

Interrelationships of these steps are shown in the CMOS/SOS Mask Fabrication block diagram of Figure 3.

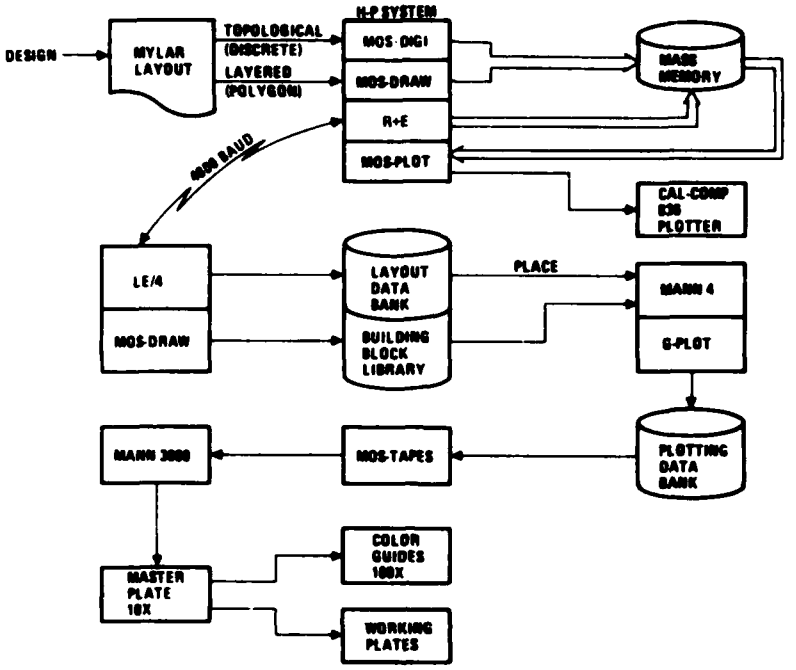


Figure 3. CMOS/SOS Mask Fabrication

2.4 DEVICE DESIGN REQUIREMENTS

Device design requirements imposed on the final design were:

1. Starting material doping, N_D, will be limited to five concentrations, 10^{14}, 10^{15}, 10^{16}, 10^{17}, 5×10^{17} atom/cm^3.

   Substrate doping concentrations were obtained by ion implantation. The amount of implant dose used for each doping level was determined from the relationship

   $$D = NKt$$

   where

   D = dose, cm^{-2}

   N = impurity concentration, atom/cm^3

   K = 0.33 - 0.35

   t = silicon thickness, cm

The 10^{14} atom/cm^3 wafer did not receive any ion implant as 10^{14} atom/cm^3 is the intrinsic value of the silicon epitaxial layer.

2. A structure to measure the doping level of the substrate is provided.

   This structure is described in Figure 4. Doping level is determined by measuring the resistance of the test structure, calculating the resistivity from the physics of the structure:

$$\rho = \frac{R(t_{si}W)}{L}$$

   where

   R = resistance in ohms

   t_{si} = silicon thickness, cm

   W = structure width, cm

   L = structure length, cm.

   and finding the corresponding impurity concentration from a graph of resistivity versus impurity concentration such as the graph in Figure 5. The initial epitaxial silicon thickness was 0.6 micron, but processing of the wafers resulted in some of the silicon being consumed. Thus, by the end of the processing, perhaps 0.4 micron of silicon remains.

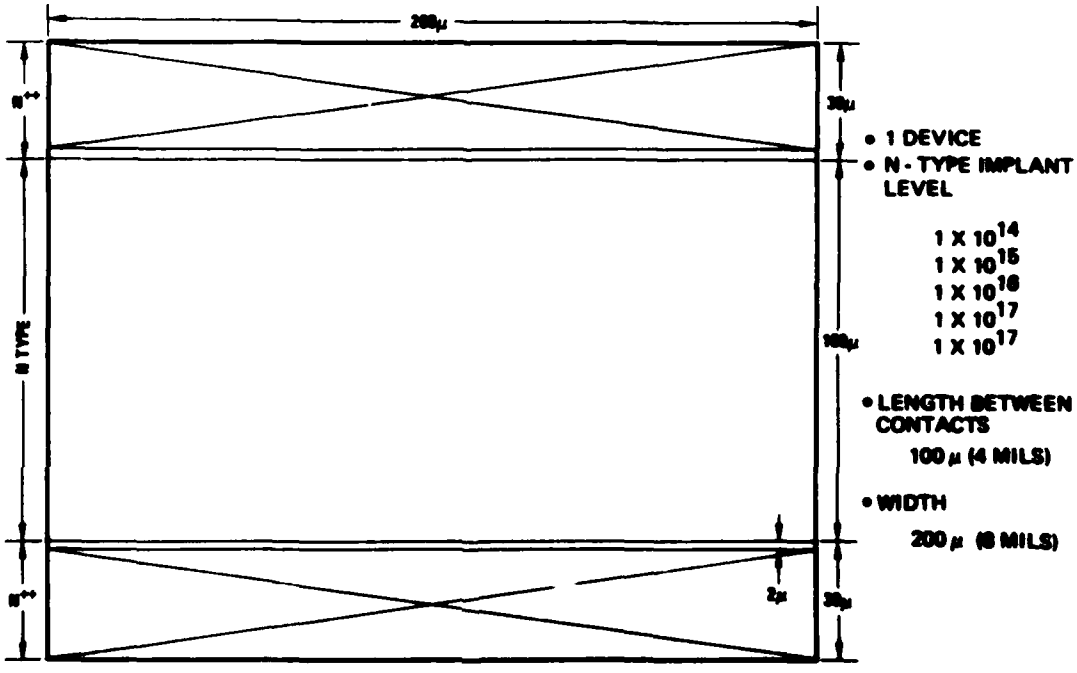


Figure 4. Doping Level Test Structure

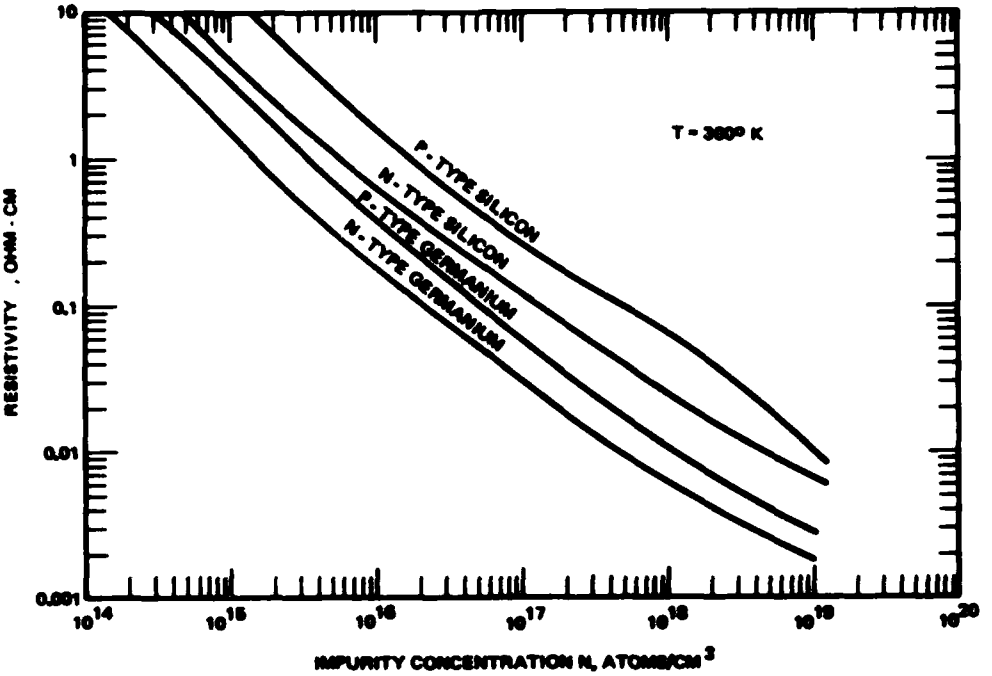


Figure 5. Resistivity as a Function of Impurity Concentration

Another factor which could affect the measurement is the presence of surface charge. An attempt to reduce the effects of surface charge was made by performing an hydroflouric acid etch of a test chip from each doping level to remove the oxide. The measurements were repeated immediately with no noticeable differences. Thus surface charge effects were excluded as a consideration from the resistivity measurements. The doping level test structure was not useful with wafer Lot 1 because a mask error resulted in no contact being made to the N^{++} regions. Use of the twenty mil diode as a substitute and other measured parameters indicated that all wafers were within a factor of two of the targeted doping levels.

A mask correction overcame this problem for wafer Lot 2. The doping level test structure indicated doping impurity concentrations as listed in Table 1.

Wafer 2 showed a marked difference between the left 1/3 and the right 2/3 of the wafer. This was most likely due to an implanter misalignment.

3. A "no defect" standard reference structure will be included for baseline comparison purposes.

This structure is described in Figure 6.

Table 1. Wafer Lot 2 - Impurity Concentrations

Wafer	Impurity Concentration (atom/cm^3)
1	10^{14}
2 Right 2/3	3×10^{14}
2 Left 1/3	10^{15}
3	10^{16}
4	10^{17}
5	5×10^{17}

4. Edge-type diodes are to be the preferred structure, but some enclosed structures will be included.

   Geometric edge effects on hot spot nucleation will be studied by including a set of Enclosed Reference Structure devices (Figure 7) of the same dimensions as the standard reference structures.

5. Diodes of 20 mil junction width will be included for experimental continuity with previous work done at Auburn University.

6. Separation of p^{++} and n^{++} regions, X_E, will have five values, 10, 30, 100, 300 and 500 microns.

   The range of lengths of the n region was selected to represent the smaller geometry devices (10 microns at one end) to a length sufficient to prevent punch through at the test pulse biases (500 microns at the long end).

7. Diode metal-to-metal spacing will be at least 3 mils, where practical. (Note: This dimension will be about 2.4 mils on devices with X_E = 10 m.)

8. Production fabrication problems resulting in metal contact spikes extending into the diffused regions or diffusion spikes extending from one diffused region into another may affect the initiation of second breakdown. Considerable attention was given to the spike design and its unique implementation into mask design and mask fabrication. This concern is indicated by the quantity of items listed regarding spike design.

   Spikes, both metal and diffusion type will be described as follows:

   - Single spikes will be included on both p^{++}, n and n^{++}, n junctions.
   - Metal spikes will not overlap the p^{++}, n or n^{++}, n junctions.
   - Metal spikes will extend from the contact into the p^{+} or n^{+} regions.
   - Spike shape is to be 60 degrees equilateral triangle, as shown in Figure 8.

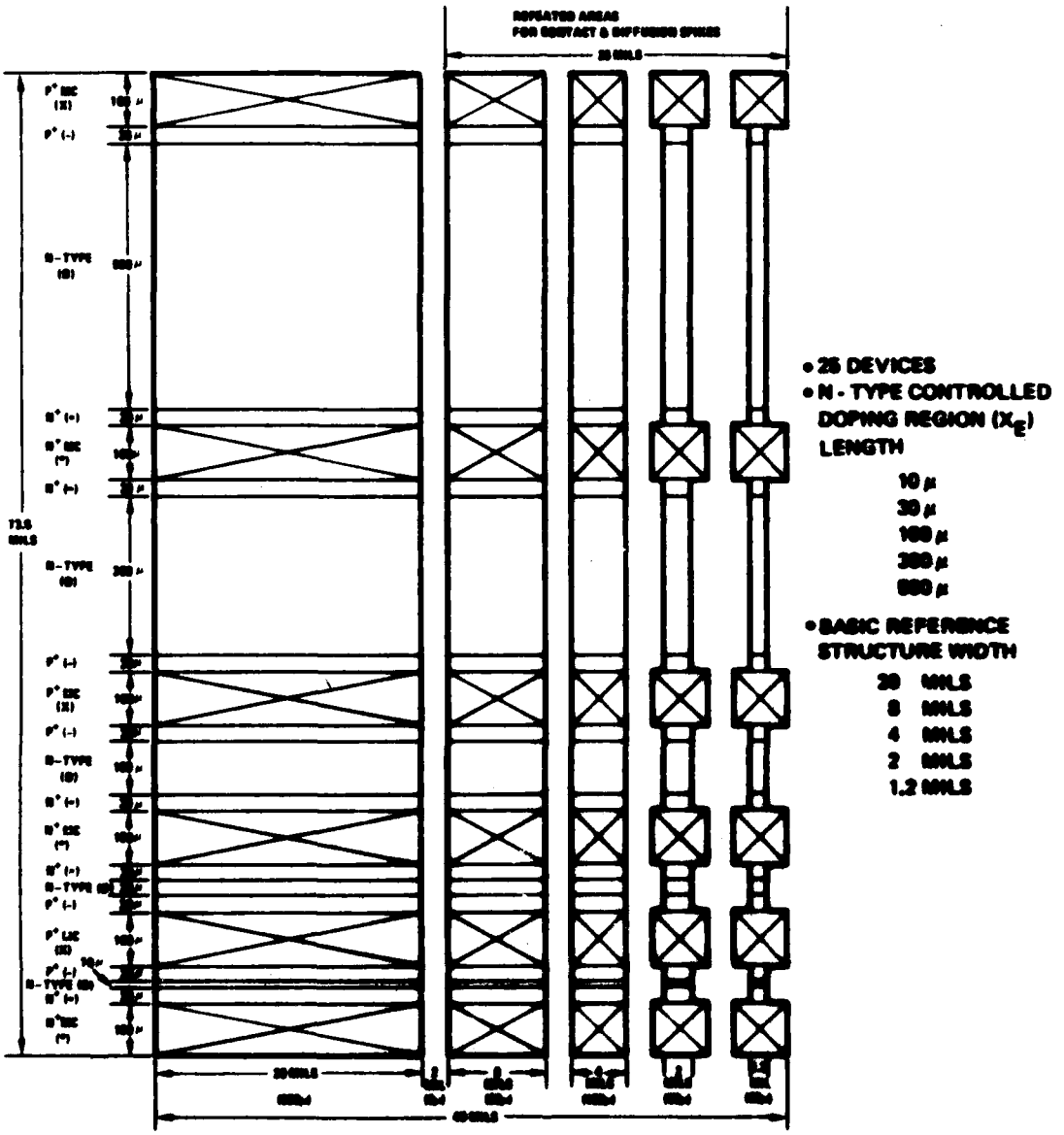
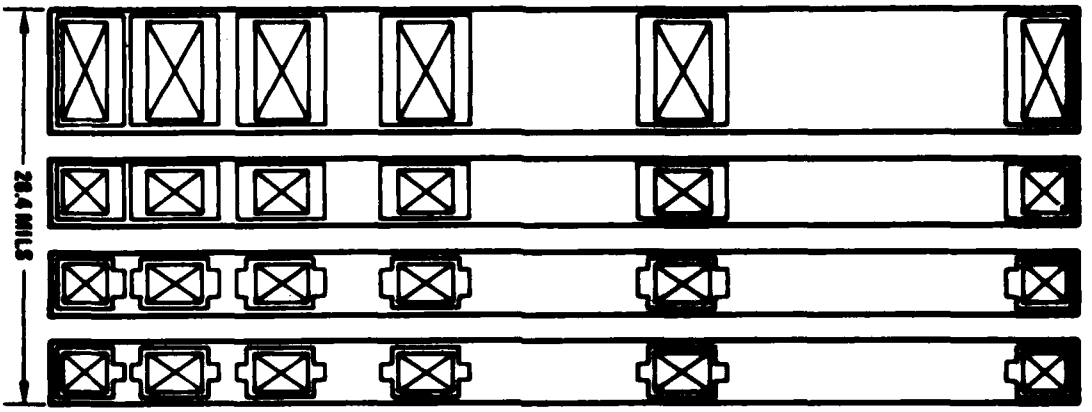


Figure 6. Standard Reference Structures



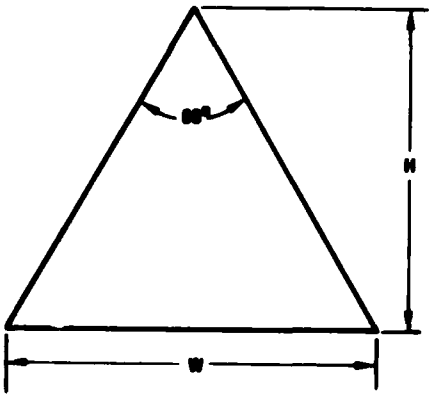
- 20 DEVICES
- N - TYPE CONTROLLED DOPING REGION (X_E) LENGTH
  - 10 μ
  - 30 μ
  - 100 μ
  - 300 μ
  - 500 μ
- BASIC REFERENCE STRUCTURE WIDTH
  - 8 MILS
  - 4 MILS
  - 2 MILS
  - 1.2 MILS

Figure 7. Enclosed Reference Structure

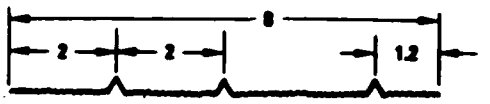
A full diode complement will consist of a set of diodes of widths 1.2, 2, 4 and 8 mils. The 8 mil width will be the standard width diode on the chip.

- There will be one full diode complement of spikes using a five-micron height.
- There will be one full diode complement of spikes using a two-and-one-half micron height.
- Multiple spikes will be designed to have 1, 2, 4, and 8 micron heights, with the one-micron spikes located sawtooth-wise across the entire junction and the 2, 4 or 8 micron spikes located as shown in Figure 8. All multiple-spike diodes will be 8 mils wide, with X_E = 10, 30 and 100 microns. Details of multiple spike construction are depicted in Figure 8.
- A minimum of 1-mil separation will be allowed between spikes and sharp contours, edges, metal, etc.
- Single spikes will be located one-fourth of the distance from the diode edge.
- The spikes will be fabricated with a point of approximately one micron diameter (minimum dimension, because of lateral diffusion limits). Eighty single-spike devices as described in Figure 8 will be included on the Standard Reference Structure type of diodes in Figure 6 to

study their effects in this regard. An attempt to determine the effects of spike size will be implemented by including a set of one-half size spikes on 20 devices as described in Figure 9. Finally, a set of diodes containing multiple spikes in combination as shown in Figure 8 is arranged according to the description of Figure 10, "Multiple Spike Structures". The 1-micron sawtooth edge is included to represent a non-smooth p-n junction or metal edge. Larger spikes are placed in areas where hot spot nucleations probably would not normally occur.



(A) SPIKE SHAPE, $W = \frac{2\sqrt{3}}{3} H$



(B) MULTIPLE SPIKE LOCATIONS ON JUNCTION. (DIMENSIONS IN MILS)

(C) MULTIPLE SPIKE CONSTRUCTION DETAIL. H = 2, 4 OR 8 MICRONS

- 80 DEVICES
- N - TYPE CONTROLLED DOPING REGION (X_E) LENGTH

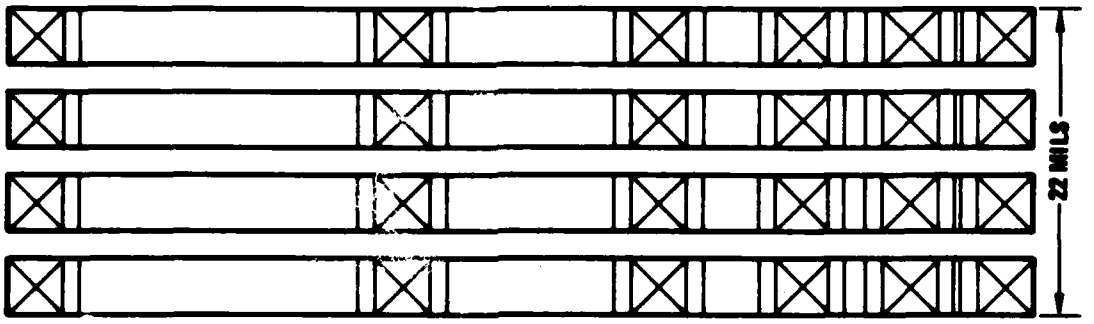
  10μ
  10 μ
  30 μ
  100 μ
  300 μ
  500 μ
- BASIC STRUCTURE WIDTH

  8 MILS
  4 MILS
  2 MILS
  1.2 MILS
- SPIKE LENGTHS — LOCATION

  5 μ — ½ DISTANCE FROM LEFT HAND ISLAND EDGE
- SPIKE DIRECTION

N^{++} CONTACT	N - TYPE	N^{++} DIFFUSION	N - TYPE
P^{++} CONTACT	N - TYPE	P^{++} DIFFUSION	N - TYPE

Figure 8. Spike Detail



- 20 DEVICES
- N - TYPE CONTROLLED DOPING REGION (X_E) LENGTH
  - 10 μ
  - 30 μ
  - 100 μ
  - 300 μ
  - 500 μ
- BASIC STRUCTURE WIDTH
  - 4 MILS
- SPIKE LENGTHS
  - 2.5 μ
- SPIKE DIRECTION

N^{++} CONTACT ➨ N - TYPE	N^{++} DIFFUSION ➨ N - TYPE
P^{++} CONTACT ➨ N - TYPE	P^{++} DIFFUSION ➨ N - TYPE

LOCATION

1 MIL FROM LEFT - HAND EDGE

Figure 9. Half-Size Spike Structure

9. Structures to simulate bipolar transistor emitter current behavior as a function of radius of curvature are included.

   Features of this cross-sectional simulation are listed and shown in the topological layout of Figure 11.

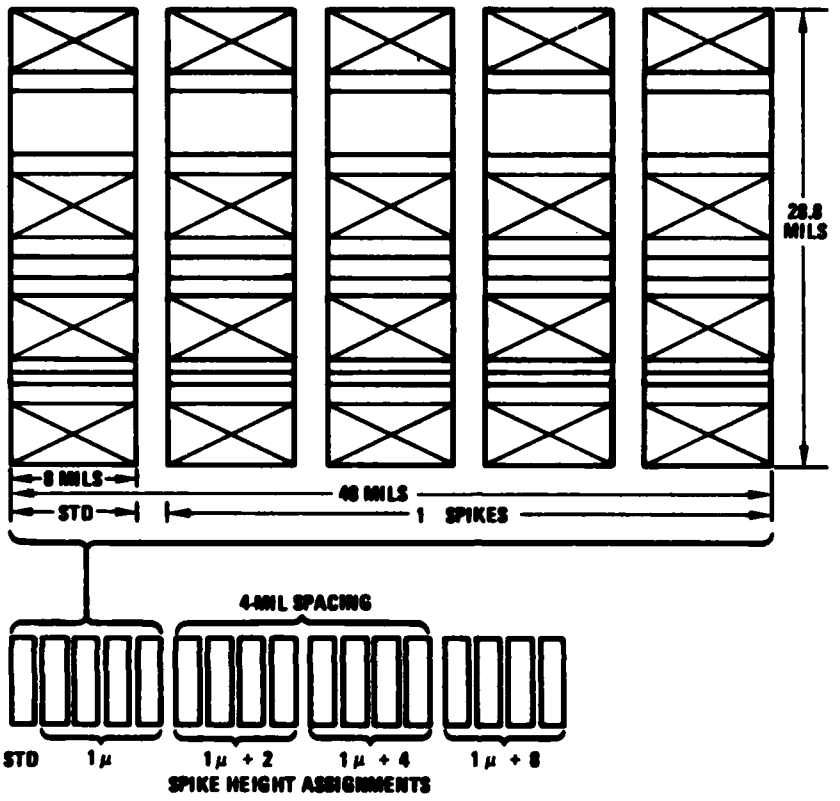
10. A four-pad structure is included to study cross current crowding effects. That is, the effects of a cross current in the N region of the diode while the current pulse is being applied between the N^{++} and P^{++} regions. This structure is described in Figure 12.

11. Simulated interdigitated structures, as shown in Figure 13 are included. This structure simulates a cross section of an interdigitated device as illustrated in Figure 14. This device is provided to enable study of laterial junction effect on hot-spot nucleations.

12. Metallization bonding pads will be 4 mils x 4 mils square. Although smaller pads could be used, this size allows reasonable ease of micro probing both for electrical characterization at Rockwell International and for Auburn University's stroboscopic pulse tests.

    Design items which were considered but omitted by mutual consent were:

    - "V" notch indents - no significant effect expected.
    - 10 micron width diodes - impractically small.
    - Circular and star structures - not enough chip area available.
    - Four- to ten-pad MSU structure - Mississippi State University withdrew their request for this device.



- 51 DEVICES
- N - TYPE CONTROLLED DOPING REGION (X_E) LENGTH

  10 μ
  30 μ
  100 μ
- BASIC STRUCTURE WIDTH

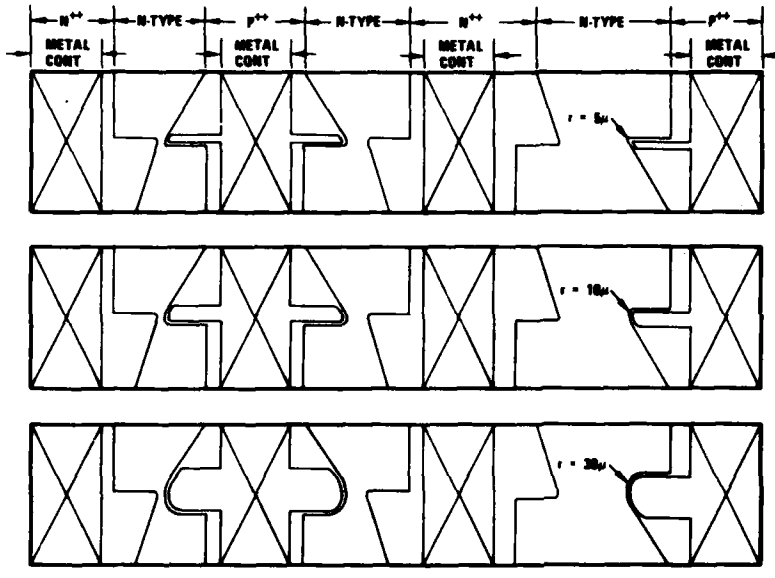
  8 MILS
- SPIKE LENGTH

1 μ	LOCATION
2 μ	CONTINUOUS ACROSS DEVICE
2 μ	2 MIL, 4 MIL, & 6.8 MIL FROM LH EDGE
4 μ	2 MIL, 4 MIL, & 6.8 MIL FROM LH EDGE
8 μ	2 MIL, 4 MIL, & 6.8 MIL FROM LH EDGE

- SPIKE DIRECTION

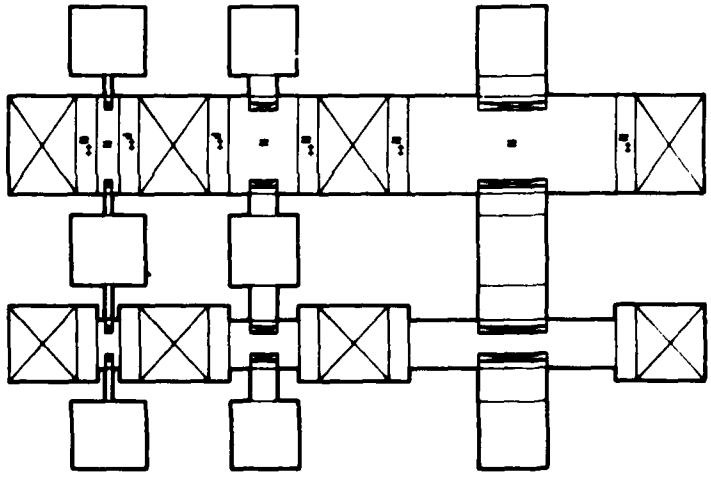
N^{++} CONTACT → N - TYPE	N^{++} DIFFUSION → N - TYPE
P^{++} CONTACT → N - TYPE	P^{++} DIFFUSION → N - TYPE

Figure 10. Multiple Spike Structures



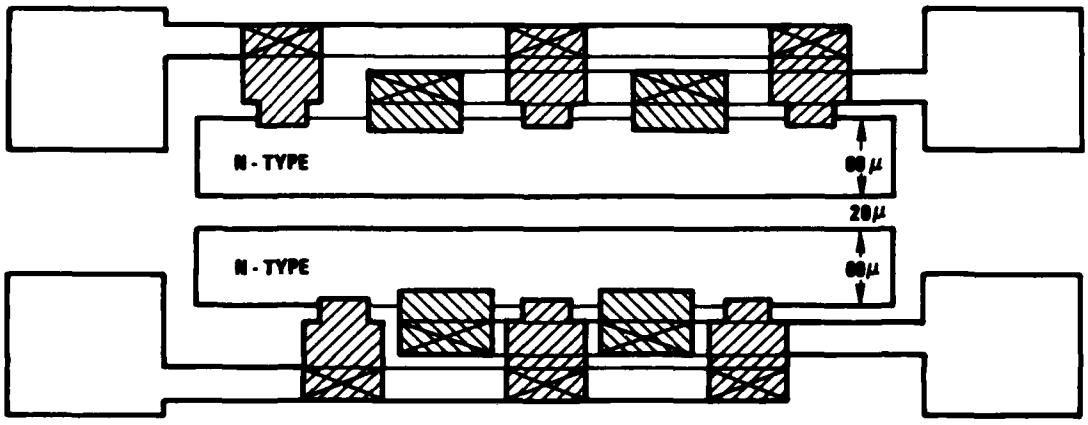
- 9 DEVICES
- RADIUS ON P^{++} DIFFUSION
  - 5 μ
  - 10 μ
  - 30 μ
- RADIUS ON N^{++} DIFFUSION
  - 5
- RADIUS SEPARATION
  - 10 μ
  - 30 μ
  - 100 μ
- CONTACT OPENING FROM P^{++} DIFFUSION EDGE
  - 5 μ
- METAL OVERLAP OF CONTACT
  - 2 μ

Figure 11. Radius of Curvature Structure



- 6 DEVICES
- N - TYPE CONTROLLED DOPING REGION (X_E) LENGTH
  - 30 μ
  - 90 μ
  - 300 μ
- BASIC STRUCTURE WIDTH AT CONTROL POINTS
  - 1.2 MIL
  - 4 MIL
- EQUAL SPACING BETWEEN CONTROL REGIONS AND CONTACT REGIONS

Figure 12. Four Terminal Structure



- 2 DEVICES
- N^{++} DIFFUSION LENGTH 5μ
- P^{++} DIFFUSION LENGTH 10μ
- N^{++} DIFFUSION WIDTH 30μ
- P^{++} DIFFUSION WIDTH 60μ
- N^{++} - P^{++} DIFFUSION SEPARATION
  - DEVICE #1: 40μ
  - DEVICE #2: 20μ
- N TYPE SEPARATION 20μ

Figure 13. Interdigitated Device

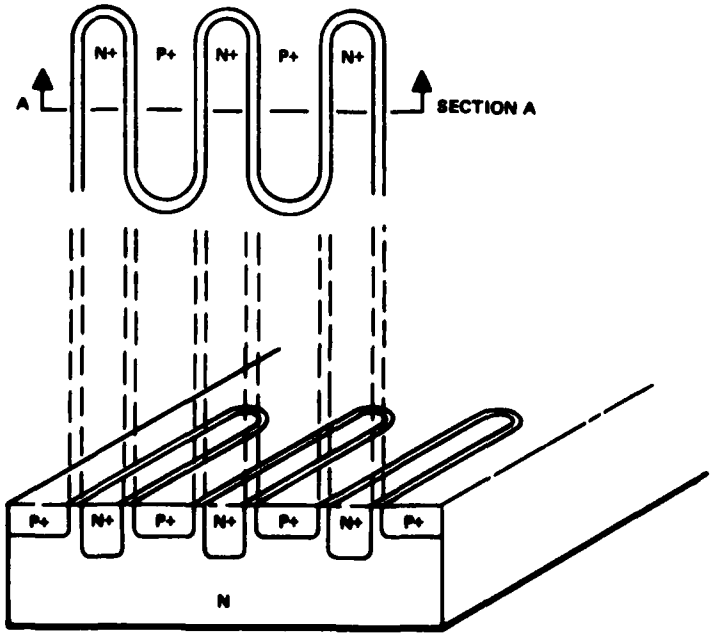


Figure 14. Origin of Simulated Interdigitated Structure

2.5 WAFER FABRICATION

Following chip device designs and mask design and fabrication, the wafers were ready for actual fabrication processing.

Special consideration was given to the preparation of SOS starting-material wafers in view of the optical requirements of the stroboscopic second breakdown tests to be performed at Auburn University.

1. The backside of the sapphire substrate was polished optically smooth.

2. To facilitate determination of top vs bottom of the wafers, a special second flat ground on each wafer as shown in Figure 15.

3. An intrinsic epi layer of silicon (0.55 to 0.65 microns thick) was doped at Rockwell International by ion implantation to obtain the five starting material doping levels.

   All wafers were sliced from a single boule.

Consideration was given to using 2-micron thick epi silicon layers to minimize current crowding effects. However two factors made use of a thicker epi layer unattractive:

1. Thicker epi layers result in less transparency. This fact impacts the Auburn University tests.

2. Increasing the epi thickness would introduce a new variable (additional yield risk) into the SOS device-fabrication process.

2.5.1 Diffusion Doping vs Ion Implantation

In the interest of keeping the series resistance of the n^{++} and p^{++} regions as low as possible, the diffusion doping method (~25Ω/□ and ~100 Ω/□, respectively) is preferred over the ion implantation method (~200 Ω/□ and ~400 Ω/□, respectively). Diffusion doping was used for forming both p^{++} and n^{++} areas.

2.5.2 Processing Steps

An outline of the SOS Electrical Overstress Processing Steps used to fabricate this chip is listed sequentially in Figure 16 Si-Gate CMOS/SOS process. It should be noted that, following step L, a doped silox passivation layer is deposited and the pad areas etched for electrical contacts.

Also, this set of processing steps is necessary to fabricate both n channel and p channel transistors on the process evaluation test pattern. Only Steps A through E actually apply to the fabrication of the diodes to be used in second breakdown tests.

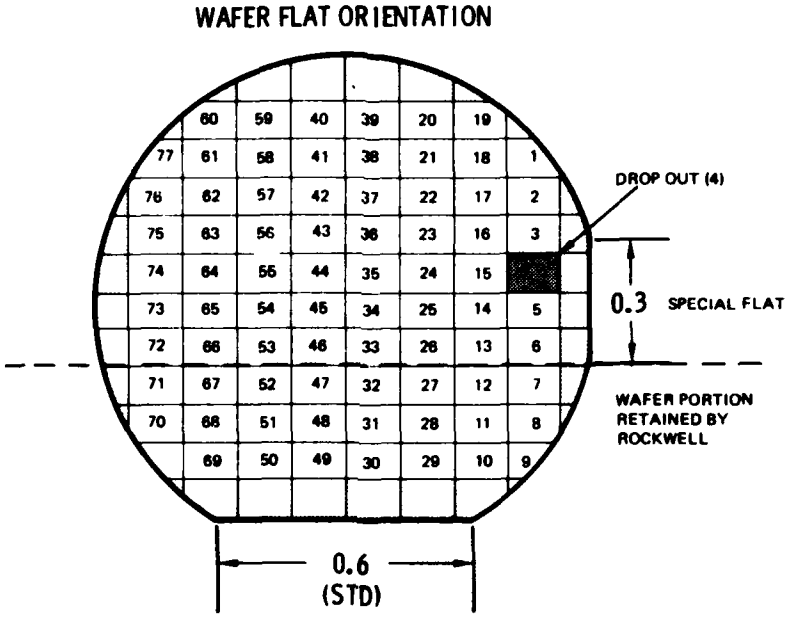


Figure 15. Die Identification

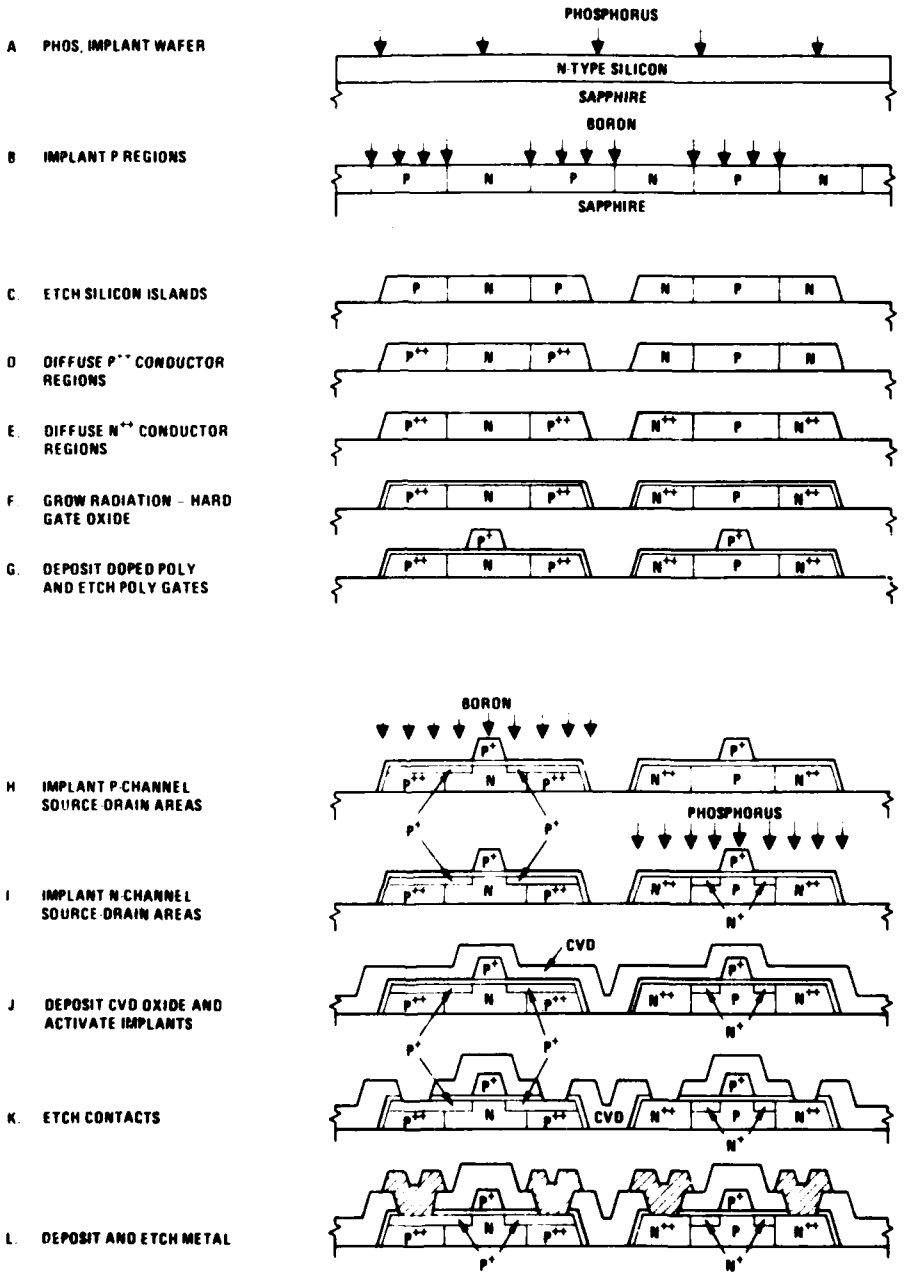


Figure 16. Si-Gate CMOS/SOS Process

2.6 DEVICE ELECTRICAL CHARACTERIZATION

Generally, two sets of electrical data are taken from five die samplings per wafer. The first data set is taken from the ten pad test pattern commonly identified as the Test 10 pattern. Most of the data taken from the Test 10 pattern is obtained using a computer programmed test. The other data set is taken from the SOS diodes and test structures using a hand microprobe and curve tracer (Tektronix 576).

2.6.1 Test 10 Electrical Characterization

The first set of data is the computerized program data obtained by probing the Rockwell Test 10 pattern. Figure 17 is a sample of the computer printout generated during this probe. At least five of these printouts were taken for each wafer. Table 2 of wafer Lot 1 and Table 3 of wafer Lot 2 are condensations of this data with averages. These averages are listed in Tables 4 and 5, Lots 1 and 2, respectively, Processing Test Pattern Data Summary. Rapid wafer-to-wafer data comparison is obtained from these tables.

These data generally referred to as "Test 10" data, are not identifiable to the die level. However, the probe pattern for these tests includes one centrally located die and one die each from the four points of the compass.

Immediately upon receipt of a wafer lot, each wafer was probed to obtain a C-V plot. The maximum capacitance value obtained from this plot was entered into a computer program (CAPAN) to determine the gate oxide thickness, t_{ox}. This value is found from the mathematical relationship between C_{ox} and t_{ox}, vis,

$$C_{ox} = \frac{K\epsilon_o A}{t_{ox}}$$

where

$K = 3.85$ for thermal SiO_2 grown in dry 0_2.

$\epsilon_o = 8.85 \times 10^{-12}$ fd/M

$A = 10$ mil $\times$ 10 mil = capacitor area

thus,

$$t_{ox} = \frac{2.2 \times 10^4}{C_{ox}} \text{ Å} \quad \text{with } C_{ox} \text{ in picofarads}$$

T_{ox} data were entered into a second computer program as the wafer processing test pattern (TST10) was being probed. Data obtained from the Test 10 program included:

```
ENTER OXIDE THICKNESS(I) ?8000
ENTER RESISTANCE SQUARE ?21.8
STARTING DEVICE NUMBER X,Y ?1,7
IS IT A AUTOMATIC TEST (1=YES; 0=NO) ?0
TEST (1=BEGIN; 0=DISCONTINUE) ?1
READY TO START TEST DEVICE NO.   1   7
METAL CONTINUITY  0.200E+00 = 4.18%
N+ / P+ RESISTANCE/SQ.  0.129E+02  0.811E+02
GATE PROTECTION DIODE  0.751E-07  0.156E+02

                N-CHANNEL TRANSISTOR

GATE LEAKAGE        -0.19E-09 AMPS
DRAIN 1HAS          0.157E-06 AMP  0.151E+02 VOLTS
DRAIN 2HAS          0.222E-06 AMP  0.146E+02 VOLTS

LOW VOLTAGE PARAMETERS (VD = 0.100

VTH1    VTH2     UFE       CH L       KP          K
2.41    2.32     395.40    6.87     0.78E-05    0.87E-04

OPERATING PARAMETERS

 VD     VTH      IDL        ION
 2.01   1.99     0.20E-06   0.14E-02
 6.02   1.33     0.33E-06   0.21E-02
10.01   1.19     0.42E-06   0.23E-02
12.01   1.07     0.55E-06   0.27E-02

LONG CH. TRANSISTORS

10.02   1.70     0.29E-06   0.19E-03

                P-CHANNEL TRANSISTOR

GATE LEAKAGE        -0.24E-09 AMPS
DRAIN 1HAS          -0.510E-08 AMP  -0.190E+02 VOLTS
DRAIN 2HAS          -0.119E-07 AMP  -0.194E+02 VOLTS

LOW VOLTAGE PARAMETERS (VD = -0.102

VTH1    VTH2     UFE       CH L       KP          K
-1.45   -1.53    284.20    3.99     0.52E-05    1.00E-04

OPERATING PARAMETERS

 VD     VTH      IDL        ION
-2.01   -1.44    -0.12E-06  -0.17E-02
-6.06   -1.61    -0.40E-06  -0.25E-02
-10.03  -1.55    -0.80E-06  -0.30E-02
-12.02  -1.50    -0.92E-06  -0.30E-02

LONG CH. TRANSISTORS

-10.03  -1.52    -0.22E-06  -0.20E-03
```

Figure 17. CMOS/SOS Test 10 Electrical Characterization

Table 2. Lot 1 Test 10 Data (Sheet 1 of 3)

Wafer 1,2										
	nA at 20V I_{GLN}	At 10 μA BV_N	V_{TN}	nA at 12V I_{LN}	mA at 18V I_{ONN}	At 10 μA BV_P	V_{TP}	nA at -12V I_{LP}	mA at -18V I_{ONP}	nA at 20V I_{GLP}
1	0.33	--	--	--	--	-21.1	-1.63	5.0	2.5	0.017
	0.20	--	--	--	--	-19.0	-0.73	--	3.1	0.043
	0.33	--	--	--	--	-19.0	-1.34	140.00	3.3	0.200
	0.27	20.7	2.47	420	2.8	-20.7	-2.03	5.7	1.8	0.190
	0.33	11.0	0.25	1.4×10^5	7.8	-25.0	-1.36	110.00	3.1	0.220
AVG	0.29	15.8	1.36	--	5.3	-21.0	-1.42	65.2	2.8	0.134
	Wafer No. 1 metal continuity = 4.38Ω; t_{ox} = 690Å									
2	0.35	23.4	4.19	140	0.58	-23.3	-2.11	6.3	0.79	0.26
	0.27	23.4	--	--	2.80	-23.0	-2.09	5.0	0.93	0.23
	0.36	23.4	2.14	220	1.50	-23.0	-2.09	6.4	0.91	0.20
	0.34	23.4	3.11	110	0.86	-23.1	-1.49	5.7	0.82	0.19
	0.34	22.5	6.13	120	0.37	-23.3	-2.90	4.4	0.88	0.25
AVG	0.33	23.2	3.89	147.5	1.20	-23.1	-2.14	5.6	0.83	0.23
	Wafer No. 2 metal continuity = 4.22Ω; t_{ox} = 628Å									

Low Voltage Parameters (V_D = 0.1V)										
	V_{TN}	μ_N	L_N	KP_N	K_N	V_{TP}	μ_P	L_P	KP_P	K_P
1	--	--	--	--	--	-2.47	152.3	5.37	3.8 E-6	5.3 E-5
	--	--	--	--	--	-2.23	138.2	4.43	3.4	5.9
	--	--	--	--	--	-2.20	142.7	5.74	4.7	6.3
	4.58	247.7	5.45	6.1 E-6	8.5 E-5	-2.86	122.0	5.90	3.0	3.9
	2.53	312.4	3.28	7.7	18.0	-2.24	143.9	4.47	3.5	6.8
AVG	3.55	280.0	4.35	6.9 E-6	1.3 E-4	-2.48	149.8	5.18	3.7 E-6	5.5 E-5
2	7.98	--	--	--	--	-4.87	--	--	--	--
	1.88	115.5	6.18	3.1 E-6	3.9 E-5	-3.82	--	--	--	--
	4.32	117.8	5.89	3.2	4.1	-3.82	--	--	--	--
	6.07	96.5	3.84	2.8	5.5	-4.71	--	--	--	--
	7.29	--	--	--	--	-5.53	--	--	--	--
AVG	5.33	109.9	5.21	3.8 E-6	4.5 E-5	-4.61	--	--	--	--

Table 2. Lot 1 Test 10 Data (Sheet 2 of 3)

Wafer 3A										
	nA at 20V I_{GLN}	At 10 μA BV_N	V_{TN}	nA at 12V I_{LN}	mA at 10V I_{ONN}	At 10 μA BV_P	V_{TP}	nA at -12V I_{LP}	mA at -10V I_{ONP}	nA at 20V I_{GLP}
3	0.54	11.1	0.00	1.2 E-5	0.7	-20.6	-1.50	10.0	3.1	0.65
	0.55	---	---	---	---	-22.1	-0.07	---	4.5	0.83
	0.57	---	---	---	---	-20.9	-0.85	4900	3.8	1.00
	0.57	---	---	---	---	-22.0	-1.38	31.0	3.6	0.74
	0.58	11.8	-3.91	1.0 E-5	0.3	-25.0	-1.53	0.1	3.2	0.68
AVG	0.56	11.4	---	1.1 E-5	0.5	-22.1	-1.07	1237	3.6	0.94
Wafer No. 3 metal continuity = 4.23Ω; t_{ox} 788Å										
4	0.240	21.8	0.12	61.0	0.73	-22.1	-1.37	3.3	1.2	0.015
	0.092	20.3	4.45	110.0	0.85	-21.9	-1.36	3.5	1.4	0.033
	0.190	---	---	---	---	-18.7	---	---	2.5	0.310
	0.075	25.0	---	---	2.30	-22.8	-1.27	3.4	1.5	0.110
	0.140	20.3	2.19	61.0	0.57	-21.7	-1.30	4.2	1.3	0.130
	0.100	22.0	4.24	68.0	0.62	-22.4	-2.10	5.6	1.3	0.150
AVG	0.140	22.0	4.25	75.0	1.00	-21.8	-1.36	4.0	1.5	0.125
Wafer No. 4 metal continuity = 4.06Ω; t_{ox} = 725Å										

Low Voltage Parameters (V_D = 0.1V)										
	V_{TN}	μ_N	L_N	KP_N	K_N	V_{TP}	μ_P	L_P	KP_P	K_P
3	2.72	746.1	9.51	1.8 E-5	1.3 E-4	-2.31	267.5	6.27	5.3 E-6	6.5 E-6
	---	---	---	---	---	-1.57	368.0	9.00	7.9	6.7
	---	---	---	---	---	-2.24	552.8	11.40	12.0	8.0
	---	---	---	---	---	-2.34	298.2	5.21	5.5	8.1
	2.68	748.4	10.20	1.8	1.2	-2.31	266.2	6.01	5.3	6.7
AVG	2.70	746.2	9.85	1.8 E-5	1.2 E-4	-2.15	334.1	7.00	7.2 E-6	7.2 E-6
4	6.04	160.8	5.63	3.7 E-6	5.1 E-6	-3.50	74.8	4.16	1.8 E-6	3.2 E-6
	5.90	---	---	---	---	-3.07	90.0	5.60	2.3	3.1
	---	---	---	---	---	-2.31	292.4	---	6.8	3.8
	5.48	160.0	3.70	4.4	6.9	-3.06	126.9	6.72	3.0	3.4
	---	---	---	---	---	-3.14	70.6	5.26	1.9	2.7
	6.12	148.0	6.04	3.6	3.1	-3.00	112.0	6.00	2.6	2.0
AVG	6.03	160.2	6.02	3.9 E-6	5.7 E-6	-3.03	131.0	5.74	3.1 E-6	3.2 E-6

Table 2. Lot 1 Test 10 Data (Sheet 3 of 3)

Wafer 5										
	nA at 28V I_{GLN}	At 10 μA B_{VN}	V_{TN}	nA at 12V I_{LN}	mA at 10V I_{ONN}	At 10 μA BV_P	V_{TP}	nA at -12V I_{LP}	mA at -10V I_{ONP}	nA at 28V I_{GLP}
5	0.48	22.5	2.56	188.0	3.1	-22.3	-1.36	2.1	1.8	0.52
	0.49	21.1	3.49	118.0	2.3	-22.8	-2.12	3.1	1.8	0.52
	0.47	21.9	4.12	42.0	0.7	-23.3	-2.16	4.7	1.2	0.53
	0.57	21.4	3.53	68.0	2.5	-22.5	-1.81	2.8	2.2	—
	0.57	20.9	3.87	37.0	2.1	-22.2	-1.59	3.5	2.0	0.55
	0.54	—	—	—	—	—	—	—	—	0.52
AVG	0.52	21.4	3.47	87.4	2.1	-22.6	-1.77	3.2	1.8	0.53
Wafer No. 5 metal continuity = 4.12Ω; t_{ox} = 683Å										

	V_{TN}	μ_N	L_N	K_{PN}	K_N	V_{TP}	μ_P	L_P	KP_P	K_P
5	3.82	168.4	5.43	4.7 E-6	6.6 E-5	-3.00	118.1	5.16	2.9 E-6	4.3 E-5
	4.68	166.2	5.60	4.1	5.6	-3.00	116.7	5.06	2.8	4.1
	7.28	147.9	3.56	3.7	7.9	-3.62	109.7	6.34	2.7	3.3
	4.61	158.7	4.14	—	7.3	-2.79	104.9	4.59	2.6	4.3
	5.20	—	—	—	—	-2.96	—	3.98	1.9	4.8
AVG	5.68	165.5	4.68	4.1 E-6	6.8 E-5	-3.07	110.6	4.85	2.6 E-6	4.2 E-5

Table 3. Lot 2 Test 10 Data (Sheet 1 of 2)

Wafer 1,2										
	nA at 20V I_{GLN}	At 10 μA BV_N	V_{TN}	nA at 12V I_{LN}	mA at 10V I_{ONN}	At 10 μA BV_P	V_{TP}	nA at -12V I_{LP}	mA at -10V I_{ONP}	nA at 20V I_{GLP}
1	0.32	20.5	4.47	1000	1.3	-20.4	-0.10	4000	2.9	0.46
	0.29	14.8	4.37	4000	1.4	---	---	---	---	0.48
	0.23	18.5	3.95	800	0.9	---	---	---	---	0.39
	0.48	13.0	2.32	2200	0.9	---	---	---	---	0.41
	0.36	18.1	4.40	2300	1.2	---	---	---	---	0.43
AVG	0.34	16.9	3.72	2330	1.1	-20.4	-0.10	4000	2.9	0.43
	Wafer No. 1 metal continuity = 4.88Ω; t_{ox} = 702Å									
2	0.40	17.3	2.31	1000	3.4	-23.6	-0.67	62.0	3.1	0.43
	0.58	16.3	1.79	2000	4.3	-23.6	-0.52	45.0	3.2	0.36
	0.49	18.7	1.90	1400	4.1	-23.6	-0.77	17.0	3.1	0.34
	0.59	15.7	2.62	3200	2.7	-23.6	-0.33	400	2.8	0.26
	0.59	17.0	2.26	2000	3.1	-23.6	-0.62	14.0	2.4	0.34
AVG	0.57	17.0	2.18	2220	3.5	-23.6	-0.62	37.0	2.9	0.35
	Wafer No. 2 metal continuity = 4.86Ω; t_{ox} = 705Å									

Low Voltage Parameters (V_D = 0.1V)										
	V_{TN}	μ_N	L_N	KP_N	K_N	V_{TP}	μ_P	L_P	KP_P	K_P
1	5.55	252.0	7.90	6.1 E-6	5.9 E-5	-0.55	145.0	7.91	3.5 E-6	3.8 E-5
	6.46	163.7	3.42	4.0	8.8	---	---	---	---	---
	5.98	178.4	8.00	4.3	4.1	---	---	---	---	---
	6.73	128.9	4.20	3.1	5.7	---	---	---	---	---
	6.66	152.4	4.90	3.7	5.7	---	---	---	---	---
AVG	6.16	175.1	5.70	4.2 E-6	6.0 E-5	-0.55	145.0	7.91	3.5 E-6	3.8 E-5
2	3.27	194.0	3.71	3.7 E-6	7.6 E-5	-0.75	96.1	3.39	2.3 E-6	5.2 E-5
	2.74	132.0	2.75	3.2	8.0	-0.65	82.4	2.80	2.0	5.0
	3.84	---	---	---	---	-0.92	111.0	4.06	2.7	5.1
	4.20	---	---	---	---	-0.80	91.0	3.74	2.2	4.5
	3.42	---	---	---	---	-1.10	160.0	4.93	2.8 E-6	4.1 E-5
AVG	3.36	163.0	3.23	3.4 E-6	8.2 E-5	-0.76	0.00	3.74	2.4 E-6	4.9 E-5

Table 3. Lot 2 Test 10 Data (Sheet 2 of 2)

Wafer 4,5										
	nA at 28V I_{GLN}	At 10 μA B_{VN}	V_{TN}	nA at 12V I_{LN}	mA at 18V I_{ONN}	At 10 μA BV_P	V_{TP}	mA at -12V I_{LP}	mA at -18V I_{ONP}	nA at 28V I_{GLP}
4	0.21	19.1	2.41	766	3.5	-23.6	-0.77	42.0	3.5	0.863
	0.23	19.1	2.39	476	3.3	-23.6	-0.58	32.0	3.5	0.863
	0.47	19.2	2.27	696	3.5	-23.6	-0.49	190	3.8	0.875
	0.35	19.3	2.33	348	3.6	-23.6	-0.66	44.0	3.6	0.846
	0.26	19.4	2.11	429	4.0	-23.6	-0.56	45.0	3.7	0.839
AVG	0.30	19.2	2.26	536	3.6	-23.6	-0.62	71.0	3.6	0.856
	Wafer No. 4 metal continuity = 4.29Ω; t_{ox} = 702Å									
5	0.16	19.2	1.51	76.0	5.6	-23.6	-0.59	42000	5.6	0.094
	0.24	19.6	1.41	116	5.3	-23.6	-0.85	1900	3.6	0.11
	0.20	19.6	1.46	54.0	5.6	-23.6	-0.26	12000	5.2	0.11
	0.22	19.6	1.72	140	5.1	-23.6	-1.06	93000	5.7	0.11
	0.26	19.7	1.62	210	4.7	-23.6	-1.16	86000	4.3	0.11
AVG	0.22	19.6	1.53	116	5.3	-23.6	-0.66	46000	4.9	0.11
	Wafer No. 5 metal continuity = 4.86Ω; t_{ox} = 662Å									

Low Voltage Parameters (V_D = 0.1V)										
	V_{TN}	μ_N	L_N	KP_N	K_N	V_{TP}	μ_P	L_P	KP_P	K_P
4	---	---	---	---	---	---	---	---	---	---
	---	---	---	---	---	---	---	---	---	---
	3.48	---	---	---	---	-0.70	---	---	---	---
	3.43	---	---	---	---	-0.95	---	---	---	---
	2.76	---	---	---	---	-0.75	---	---	---	---
AVG	3.19	---	---	---	---	-0.80	---	---	---	---
5	2.30	144.2	1.46	3.7 E-6	2.8 E-4	-0.30	132.4	3.82	3.4 E-6	8.8 E-6
	2.44	164.2	1.92	4.2	1.7	-0.36	129.8	5.15	3.3	4.9
	2.34	163.5	1.92	4.7	1.9	-0.83	119.9	2.90	3.1	7.9
	2.66	193.7	2.06	5.0	1.6	-0.71	127.2	3.82	3.3	8.3
	2.63	207.6	3.06	5.3	1.3	-0.62	133.9	4.70	3.4	5.5
AVG	2.49	178.8	2.17	4.8 E-6	.7 E-4	-0.46	128.6	3.70	3.3 E-6	7.0 E-6

Table 4. Lot 1 Processing Test Pattern Data Summary

Wafer	Doping Level	t_{ox} (Å)	Metal Cont. (Ω)	I_{GL} at 20V (nA)	I_{DL} at 12V (nA)	BV (10 μA)	V_T V_D = 10V	μ cm^2/V-sec	L μM	
1	10^{14}	800	4.38	0.29	*	15.8	1.36	288	4.35	
2	10^{15}	628	4.22	0.33	147	23.2	3.89	118	5.21	
3	10^{16}	788	4.23	0.56	*	11.4	*	*	*	n-Channel
4	10^{17}	726	4.86	0.14	75	22.8	4.25	186	6.82	
5	$5 \cdot 10^{17}$	883	4.12	0.52	87.4	21.4	3.47	186	4.68	
1	10^{14}	800	4.38	0.13	85.2	-21.8	-1.42	156	5.18	
2	10^{15}	628	4.22	0.23	5.6	-23.1	-2.14	*	*	
3	10^{16}	788	4.23	0.94	1238	-21.8	-2.55	334	7.88	p-Channel
4	10^{17}	726	4.86	0.13	4.8	-21.8	-1.36	131	5.74	
5	$5 \cdot 10^{17}$	883	412	0.53	3.2	-22.8	-1.77	111	4.85	

*Data not recorded by computer.

Table 5. Lot 2 Processing Test Pattern Data Summary

Wafer	Doping Level	t_{ox} (Å)	Metal Cont. (Ω)	I_{GL} at 20V (nA)	I_{DL} at 12V (nA)	B_V (10 μA)	V_T V_D = 10V	μ cm^2/V-sec	L μM	
1	10^{14}	702	4.00	0.30	2970.0	16.5	3.15	283.3	6.21	
2	10^{15}	705	4.00	0.02	2367.0	17.0	2.34	143.0	3.23	
3	10^{16}	707	3.70	0.40	1330140.3	22.4	3.22	233.1	*	n-Channel
4	10^{17}	702	4.20	0.20	536.0	19.2	2.20	*	*	
5	$5 \cdot 10^{17}$	602	4.06	0.21	131.0	19.5	1.40	190.0	2.40	
1	10^{14}	702	4.00	0.44	4600.0	20.4	-0.10	145.0	7.01	
2	10^{15}	705	4.00	0.35	227.3	-23.5	-0.56	102.0	3.06	
3	10^{16}	707	3.70	0.36	702.2	-21.0	-2.00	130.1	3.00	p-Channel
4	10^{17}	702	4.20	0.070	71.0	-23.5	-0.02	*	*	
5	$5 \cdot 10^{17}$	602	4.06	0.10	40016.0	-23.5	-0.53	120.5	3.04	

*Data not recorded by the computer.

1. Metal Continuity – a measure of resistance in a 1/4 mil wide aluminum strip traversing 16 steps. Resistance is found by measuring the voltage drop across the strip while 50 mA is applied and performing the required arithmetic. A value less than 5 Ω is acceptable.

2. Gate Leakage Current – is measured with 20 volts between the gate and channel. Values of 100 nA or greater cause the computer program to abort further tests on the device in probe.

3. Drain Leakage Current – is measured with five volts shut-off bias on the gate and 12 volts on the drain. Values of 10 μA or greater cause the computer program to abort further tests on the device in probe.

4. Drain Reverse Breakdown Voltage – is measured at 10 μA with five volts shut-off bias on the gate.

5. Threshold Voltage – is measured at a drain voltage of 10 volts. The computer utilizes a least squares fit method to extrapolate the I_d vs V_G curve to the V_G at which $I_d = 0$

6. Channel Mobility – is also found from a least squares fit method to determine the slope of the I_d vs V_G curve from which mobility is determined, vis,

$$\mu = \frac{\text{slope}}{C_{ox}}$$

These are low voltage parameters, that is $V_D = 0.1$ volts.

7. Channel Length – is computed by combining the slopes of the conductance curves obtained from the 0.3 x 3 mil and 3 x 3 mil transistors (channel width of the small device equals channel width of the large device, Z small = Z large) to obtain:

$$L\ (0.3 \times 3) = \frac{\text{slope}(3 \times 3)}{\text{slope}(0.3 \times 3)} L\ 3 \times 3)$$

or, since L (3 x 3) = 3 mil = 75 μm,

$$L\ (0.3 \times 3) = 75 \frac{\text{slope}(3 \times 3)}{\text{slope}(0.3 \times 3)},\ L \text{ in } \mu M.$$

2.6.1.1 Test 10 Data Comments

Lot 1

The generally high n-channel threshold voltages and low n-channel mobilities are a result of the poly-silicon gate material not receiving the required doping concentration due to equipment failure at this processing step. However, the function of the SOS diodes was not affected by this problem since no poly-silicon is used in the diode process.

Lot 2

A cursory inspection of the Test 10 data in Table 3 or Table 5 indicates excessive drain leakage current for both n-channel and p-channel transistors. Good values to use as standards of judgement would be $I_{DLN} \leq 50$ nA and $I_{DLP} \leq 10$ nA. Curve tracer I-V characteristics also indicate some leakage but not in the degree tabulated by the Test 10 data. Comparison of these data with the data taken from the diodes, together with a review of the processing steps, points to the problem lying in the additional implant steps required for the transistors and secondly, to the possibility of noncontiguous silox masking along the island edges during these "extra" implant steps. This combination of events can create an undesirable conduction path along the island edge. The diodes do not exhibit high leakage characteristics on any wafer so that, in this regard, the leakage problem does not pose a threat to the performance of Dr. Budenstein's second breakdown tests.

2.6.2 Diode Electrical Characterization

An identification of lot, wafer, die, structure, and component is necessary as a prelude to diode data discussion. To be compatible with BDM's Tektronix CP112 Floppy Disc recorder the following identification number has been established:

AB CC DD EE

where A is the lot number (1,2), B is the wafer number (1-5), CC is the die number (01-80), DD is the structure type (01-14), and EE is the diode number (01-51). Thus, Lot 1, Wafer 2, Die 03, structure 04, and diode 05 would appear 12030405.

Physically, the wafers will be identified by a mark in the dropout area such as 1-2, indicating Lot 1, Wafer 2. The die will be identified according to their relative position to the dropout as shown in Figure 15. Structures within each die can be located by the structure identification photograph in Figure 18. Finally, a blowup of Figure 18 allows each component to be numerically identified as shown in Figure 19, SOS Diode Identification.

The second set of data was concerned with forward and reverse characteristics of the SOS diodes. These data consisted of:

1. Diode Forward Voltage vs Forward Current. A Tektronix 576 curve tracer was used to obtain the diode I-V characteristics. V_f was measured at $I_f = 10\,\mu A$, $50\,\mu A$, $100\,\mu A$ and 1 mA or to breakdown, whichever occurred first.

2. Diode Reverse Breakdown Voltage – was also obtained from curve tracer I-V characteristics. BVD was defined in all cases at $I_R = 10\,\mu A$. If breakdown was not reached by 400 volts, then the current at 400 volts was recorded and no higher voltage was attempted.

Using the above methods, one die from a wafer in each lot was fully characterized; that is, all diodes on the die were characterized. These results are shown in Table 6 for Lot 1 and Table 7 for Lot 2 and provided some means of

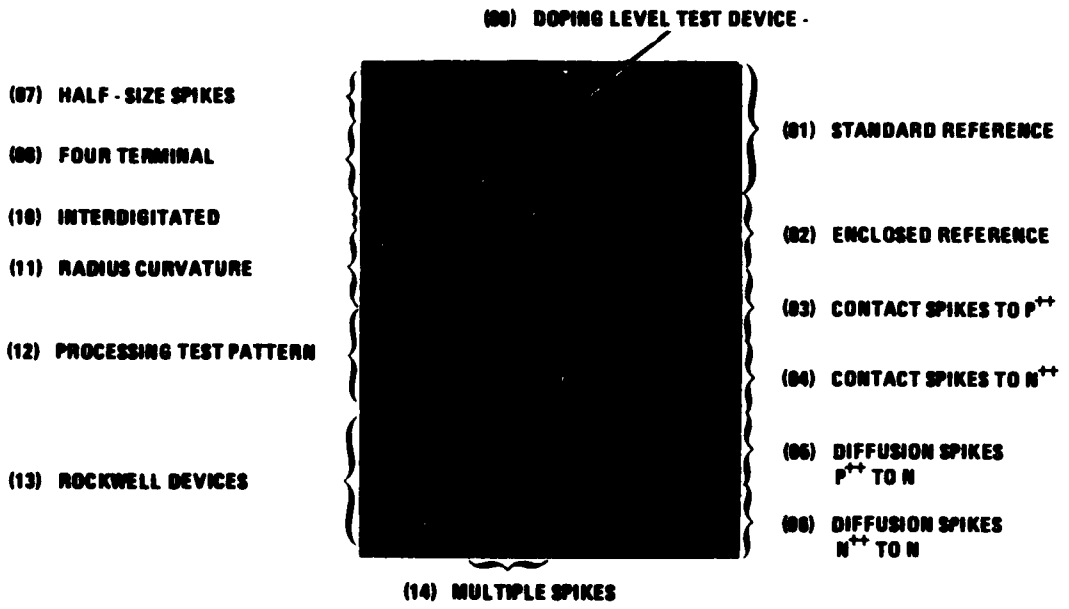


Figure 18. Structure Identification

establishing a guideline for the method of sample testing the wafer lot. From these data it was concluded to use the diodes of n-region width, $X_E = 30\ \mu M$ and diode width - 8 mils as the sample vehicle. Further, to eliminate repetition, but to gain a cross section of diode types, Structures 01, 02, 07 and 11 were selected. The data obtained from five die on each of the wafers are listed in Table 8, Wafers 1, 2, 3, 4 and 5, respectively, from Lot 1 and in Table 9, Wafers 1, 2, 4 and 5 respectively, from Lot 2. Data from Lots 1 and 2 are summarized in Tables 10 and 11 respectively, Diode Data Summary, to give a ready comparison of parameters.

A "BD" in this table means that the diode has reached breakdown. An arrow (→) means that thermal walkout was not entirely stable at the time the measurement was taken. A line means no measurement was taken.

2.6.3 Starting Doping Levels

Structure 09 is a doping level test structure consisting of a large resistor to be used to determine the starting material doping concentrations of each wafer. On Lot 1 this structure contained a mask error such that no contact was made from the metal to the N^{++} material. This error was rectified so that the doping level test structure is functional in Lot 2. Impurity concentrations determined from doping level test structure measurements are listed in Table 1 for Lot 2. Lot 1 was determined by reverse breakdown and diode body resistance measurements to be within a factor of two of the targeted values.

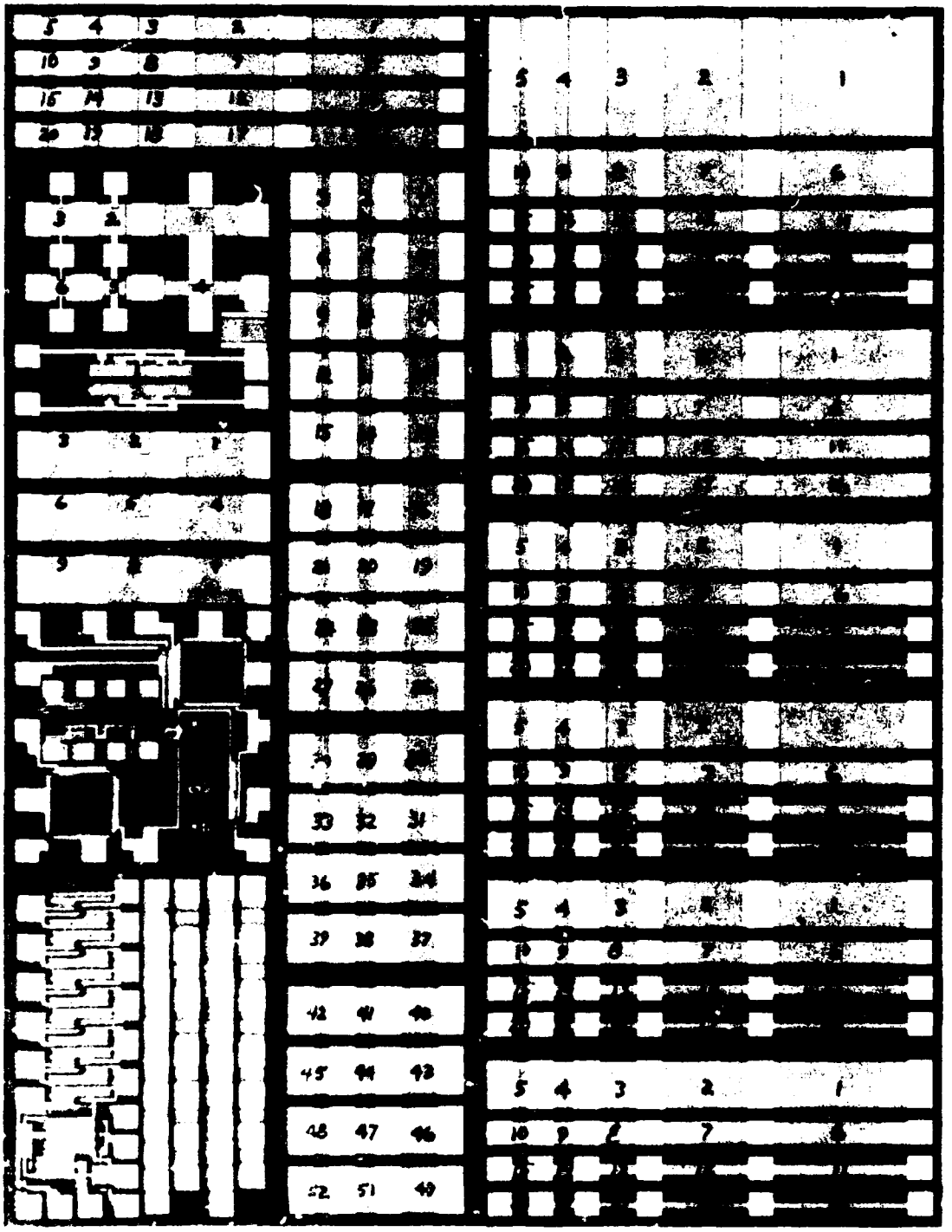


Figure 19. SOS Diode Identification

Table 6. Lot 1 Diode Electrical Characterization

Wafer 3	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 35	01	01	400 1 μA	25 2.5 MΩ resistive	68	104	--
10^{16} atoms/cm^3		02	330	6.9	39	103	--
		03	400 4 μA	2.1	9.0	19	370
		04	210	0.86	2.2	3.8	22
		05	90	0.56	1.0	1.4	4.0
		06	400 2 μA	30 3 MΩ resistive	100	350	--
		07	350	10.4	57	200	--
		08	400 2 μA	2.4	5.4	22.5	400 0.8 μA
		09	200	1.4	5.0	11.0	50 soft
		10	400 ~1 μA	0.75	1.63	2.6	4.4
		11	400 ~2 μA	130 13 MΩ resistive	400	--	--
		12	400 4 μA	60	80	100	400 0.4 μA
		13	275	25	30	40	148
		14	200 sharp	6	10	13	27
		15	98 sharp	0.9	2.0	2.9	4.3
		16	400 1 μA	140 14 MΩ resistive	275	400	--
		17	400	50	170	200	400 0.2 μA
		18	400 1 μA	65	120	160	400 0.7 μA
		19	280	11	21	28	48
		20	--	--	--	--	--
		21	400 1 μA	110 11 MΩ resistive	210	270	400 188 μA
		22	400	9.9	105	156	400 175 μA
		23	--	52	100	130	Burnout
		24	Burnout	--	--	--	--
		25	Burnout	1.5	3.2	3.7	6.4
	02	01	400 2 μA	84 8.4 MΩ resistive	400 40 μA	--	--
		02	400 2 μA	20	70	300	400 140 μA
		03	270	2.5	9.0	15.0	100
		04	134	5.5	10.0	12.2	20
		05	120 Burnout	--	--	--	--

Table 6. Lot 1 Diode Electrical Characterization (Cont)

Wafer 3	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 35	03	01	400 4 μA	64	300	400 90 μA	--
		02	300	23	92	400	--
10^{16} atoms/cm^3		03	400 4 μA	14	46	104	400 8.6 mA
		04	250	6.1	14	18.5	20.5
		05	124	3.4	4.1	4.2	4.6 BD
	04	01	400 2 μA	54	300	400 80 μA	--
		02	300	14	95	400 90 μA	--
		03	400 4 μA	17	61	130	400 8.8 mA
		04	200	5	15	23	45 BD
		05	140	3.1	4.2	4.3	4.7 BD
	05	01	400 7 μA	10.1 MΩ	300	400 80 μA	--
		02	300	15	110	400	--
		03	400 4 μA	18	75	120	400 8.7 mA
		04	230	6.4	14.8	17.8	31.8
		05	82	0.85	1.25	1.5	3.7
	06	01	400 5 μA	43	300	400 82 μA	--
		02	320	26	140	400 80 μA	--
		03	400 4 μA	16	62	140	400 50 A
		04	220	5.6	16	21	40 BD
		05	Burnout at 200V	--	--	--	--
	07	01	400 2 μA	100	250	325	400 145 μA
		02	200	17	55	110	400 180 μA
		03	400 2 μA	16	47	100	400 0.84 mA
		04	200	7	18	30	80 BD
		05	140	1.1	3.8	4.1	4.3 BD
	08	01	300	10.4	30	80	400 240 A
		02	225	8.8	25	36	Burnout
		03	100	1.6	5.6	10	44
	10	01	200	2.5	7.8	14.2	70
		02	140	1.1	3.2	6.8	30
	00	01	100 x 20 μA = 5 MΩ				

Table 6. Lot 1 Diode Electrical Characterization (Cont)

Wafer 3	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 35	11	01	350	12.2	72	250	400 200 μA
10^{16} atoms/cm^3		02	290	7.2	31	45	84
		03	Burnout	--	--	--	--
		04	400	12.1	105	270	--
		05	260	6.4	70	88	--
		06	140	3.3	5.3	6.4	18
		07	300	7.8	54	225	--
		08	250	3.4	28.5	76	90 BD
		09	140	2.2	7.3 BD	--	--
	14	01	400	6.0	25	75	400 0.5 mA
		02	180	2.0	5.8	11.6	100 BD
		03	120	0.7	1.5	2.4	4.5 BD
		04	400 4 μA	14	40	88	400 0.6 mA
		05	200	1.9	5.7	11.2	100 BD
		06	120	0.7	1.4	2.2	4.5 BD
		16	280	4.2	17.5	47	400 0.5 mA
		17	170	1.6	5.0	9.9	100 BD
		18	120	0.7	1.4	2.3	4.5 BD
		28	170	4.3	17.5	4.6	400 0.46 mA
		29	235	2.2	6.8	11.0	100 BD
		30	140	1.9	2.3	2.7	4.8
		40	400 8 μA	8.6	130	250	400 0.3 mA
		41	190	1.8	8.0	20.0	100 BD
		42	110	0.8	2.4	4.0	5 BD

Table 7. Lot 2 Diode Electrical Characterization (Full)

Wafer 5	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 35	01	01	11.80	0.56	0.70	0.82	2.60
$5 \cdot 10^{17}$		02	11.80	0.56	0.67	0.75	1.90
		03	11.60	0.55	0.62	0.67	1.10
$\frac{atom}{cm^3}$		04	4.9 soft	0.55	0.62	0.65	0.87
		05	11.60	0.54	0.60	0.63	0.76
		06	11.80	0.62	0.87	1.13	5.50
		07	12.00	0.61	0.78	0.96	3.70
		08	11.70	0.58	0.68	0.76	1.75
		09	11.90	0.58	0.66	0.70	1.10
		10	11.60	0.57	0.64	0.70	0.92
		11	11.80	0.70	1.13	1.63	10.20
		12	12.00	0.66	0.96	1.27	6.80
		13	11.80	0.62	0.76	0.88	2.70
		14	11.60	0.61	0.69	0.75	1.43
		15	11.80	0.60	0.67	0.71	1.20
		16	12.20	0.62	1.64	2.60	19.50
		17	11.80	0.74	1.27	1.90	12.40
		18	11.90	0.66	1.08	1.10	4.70
		19	11.90	0.64	0.75	0.84	2.10
		20	11.80	0.63	0.71	0.76	1.38
		21	12.20	0.97	2.30	3.90	27.00
		22	12.10	0.84	1.68	2.70	20.00
		23	12.00	0.71	1.04	1.38	7.40
		24	12.00	0.67	0.81	0.95	2.90
		25	11.80	0.65	0.74	0.81	1.60
	02	01	11.60	0.60	0.84	1.06	5.10
		02	11.60	0.58	0.76	0.93	3.50
		03	11.70	0.56	0.67	0.75	1.70
		04	11.60	0.56	0.65	0.68	1.12
		05	11.60	0.55	0.63	0.67	0.92
		06	11.80	0.65	1.04	1.40	8.00
		07	11.80	0.62	0.80	1.17	5.70
		08	11.80	0.59	0.73	0.84	2.47
		09	11.80	0.56	0.68	0.74	1.36
		10	11.60	0.57	0.66	0.70	1.02

Table 7. Lot 2 Diode Electrical Characterization (Full) (Cont)

Wafer 5	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 35	02	11	11.90	0.66	1.88	1.56	9.88
$5 \cdot 10^{17}$		12	11.0 soft	0.63	0.92	1.22	6.38
		13	11.0 soft	0.58	0.74	0.87	2.75
atom		14	11.0 soft	0.58	0.89	0.76	1.56
cm^3		15	11.0 soft	0.57	0.87	0.72	1.15
		16	11.90	0.66	1.10	1.56	9.88
		17	11.80	0.62	0.93	1.24	6.40
		18	11.70	0.58	0.75	0.88	2.98
		19	11.80	0.58	0.71	0.80	1.78
		20	11.80	0.57	0.68	0.74	1.40
	03	01	11.80	0.62	0.88	1.14	5.58
		02	11.80	0.61	0.79	0.96	3.74
		03	11.8 soft	0.58	0.68	0.76	1.72
		04	11.80	0.58	0.85	0.78	1.99
		05	11.80	0.57	0.84	0.88	0.91
	04	01	11.90	0.62	0.88	1.14	5.60
		02	11.80	0.61	0.78	0.96	3.78
		03	11.80	0.58	0.89	0.76	1.88
		04	11.80	0.58	0.86	0.70	1.12
		05	11.8 soft	0.57	0.84	0.87	0.90
	05	01	11.80	0.62	0.88	1.15	5.85
		02	11.80	0.61	0.79	0.96	3.75
		03	11.90	0.58	0.88	0.76	1.76
		04	11.80	0.58	0.86	0.71	1.16
		05	11.80	0.57	0.84	0.88	0.94
	06	01	11.90	0.62	0.88	1.15	5.84
		02	11.80	0.61	0.79	0.97	3.80
		03	11.80	0.58	0.88	0.76	1.82
		04	11.90	0.58	0.86	0.70	1.13
		05	11.90	0.57	0.84	0.87	0.88
	07	01	7.20 soft	0.69	1.13	1.82	10.20
		02	11.80	0.66	1.95	1.27	6.90
		03	11.80	0.62	0.76	0.89	2.75
		04	11.80	0.61	0.78	0.77	1.63
		05	11.20 soft	0.60	0.87	0.71	1.02

Table 7. Lot 2 Diode Electrical Characterization (Full) (Cont)

Wafer 5	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 35	08	01	11.60	0.62	0.79	0.86	3.55
$5 \cdot 10^{17}$		02	11.80	0.60	0.71	0.88	1.98
		03	11.80	0.59	0.67	0.71	1.17
atom	09	01	5V at mA = 1 KΩ				
cm^3	10	01	11.60	0.59	0.68	0.74	1.42
		02	11.60	0.59	0.67	0.73	1.38
	11	01	11.70	0.58	0.70	0.80	2.20
		02	11.60	0.58	0.67	0.74	1.56
		03	11.70	0.57	0.66	0.71	1.27
		04	11.60	0.58	0.70	0.80	2.20
		05	11.70	0.58	0.67	0.75	1.80
		06	11.80	0.57	0.66	0.72	1.32
		07	11.80	0.58	0.71	0.81	2.21
		08	11.60	0.58	0.68	0.76	1.58
		09	11.60 soft	0.57	0.66	0.72	1.31
	14	01	11.80	0.58	0.69	0.77	1.82
		02	9.20 soft	0.58	0.66	0.70	1.38
		03	11.60	0.57	0.64	0.67	0.89
		04	11.66	0.58	0.69	0.77	1.82
		05	11.70	0.58	0.66	0.71	1.18
		06	11.60	0.57	0.64	0.68	0.94
		16	9.40 soft	0.58	0.69	0.77	1.81
		17	11.80	0.58	0.66	0.70	1.16
		18	11.80	0.57	0.64	0.68	0.96
		28	11.80	0.58	0.69	0.77	1.82
		29	11.90	0.58	0.66	0.70	1.17
		30	11.30 soft	0.57	0.64	0.68	0.95
		40	12.00	0.58	0.69	0.77	1.82
		41	11.80	0.58	0.66	0.70	1.17
		42	11.80	0.57	0.64	0.68	0.95

Table 8. Lot 1 Diode Electrical Characterization

Wafer 1	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die	01	09	260V	12.0V	28.2V	33.7V	44.0V
10^{14}	02	04	250	12.0	25.0	30.0	43.0
cm^{-3}	07	04	200	21.5	63.5	74.0	90.0
04	11	02	290	20.0	32.5	40.0	66.0
		05	240	29.5	50.0	57.0	100.0
		08	270	25.0	45.5	53.0	96.0
44	01	09	220	9.5	26.0	31.0	39.0
	02	04	225	9.5	22.0	26.0	37.0
	07	04	160	17.0	45.0	54.5	73.0
	11	02	200	21.0	38.0	45.0	62.0
		05	220	21.0	40.5	47.4	65.0
		08	260	22.0	40.0	46.3	64.0
15	01	09	170	5.2	16.4	23.2	28.0 BD
	02	04	145	5.4	15.0	20.0	26.1 BD
	07	04	210	13.2	40.5	48.0	56.0 BD
	11	02	150	15.0	30.4	35.0	66.0
		05	160	16.0	33.0	37.3	60.2
		08	160	15.3	32.0	36.5	60.0
41	01	09	150	5.1	14.2	18.4	27.0
	02	04	160	4.7	11.0	15.3	26.5
	07	04	160	9.0	27.2	35.0	50.5
	11	02	140	13.0	27.0	34.0	70.0
		05	156	13.1	28.2	35.0	72.5
		08	160	11.0	26.0	32.7	60.0
32	01	09	170	9.3	26.2	31.5	39.0 BD
	02	04	215	10.1	24.0	28.7	38.1 BD
	07	04	190	20.0	56.5	63.1	78.0 BD
	11	02	200	26.5	43.0	48.0	64.0
		05	230	26.4	46.4	51.5	68.0
		08	220	24.0	43.0	47.0	62.5
Avg. of	01	09	182	8.2	22.0	27.0	36.5
5 Dio	02	04	190	8.3	19.7	24.2	34.1
	07	04	184	16.3	46.0	56.1	71.1
	11	02	196	19.2	34.5	40.4	77.0
		05	201	21.2	38.0	46.0	69.:
		08	202	19.0	37.3	43.3	70.0

Table 8. Lot 1 Diode Electrical Characterization (Cont)

Wafer 2	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 10^{15} cm^{-3}	01	03	200V	21.2V	60.7V	66.2V	72.8V SD
	02	04	245	25.7	67.8	74.1	83.8
	07	04	---	48.8	94.6	106.8	Burnout
64	11	02	280	63.8	86.8	86.8 SD	
		05	280	60.8	100.8 SD	100.8 SD	
		08	295	53.8	87.8	87.8	
44	01	03	240	27.5	65.8	67.8 SD	
	02	04	283	38.4	71.8	77.4	88.3 SD
	07	04	250	40.8	94.8	108.8	134.8 SD
	11	02	310	70.8	97.8 SD	98.8 SD	
		05	330	66.8	104.8 SD	106.8 SD	
		08	300	62.8	100.8 SD	100.8 SD	
15	01	03	220	20.4	62.7	67.5 SD	
	02	04	275	22.5	67.3	77.8	96.8 SD
	07	04	120	43.8	96.8	108.5	138.8 SD
	11	02	300	64.3	94.8 SD	96.8 SD	
		05	310	67.4	102.8 SD	104.8 SD	
		08	315	58.2	92.8 SD	92.8 SD	
41	01	03	220	20.3	57.4	64.8 SD	
	02	04	260	23.7	64.2	72.8	82.8 SD
	07	04	---	41.6	92.2	118.8	Burnout
	11	02	310	66.8	94.2 SD	94.2 SD	
		05	310	65.6	102.8 SD	102.8 SD	
		08	320	60.8	100.8 SD	100.8 SD	
32	01	03	200	30.3	62.8 SD	62.8 SD	
	02	04	200	43.2	80.8	74.8	76 SD
	07	04	245	60.8	97.8	108.8	128 SD
	11	02	295	74.4	84.8 SD	84.8 SD	
		05	320	70.8	80.8 SD	92.8 SD	
		08	325	76.5	86.8 SD	86.8 SD	
Avg. of 5 Die	01	03	232	25.7	61.6	66.5 SD	72.8 SD
	02	04	268	30.7	67.7	74.8	82.1 SD
	07	04	286	48.8	95.2	108.3	136.5 SD
	11	02	290	68.1	91.4 SD	92.8 SD	
		05	310	36.8	98.4 SD	100.8 SD	
		08	323	66.3	93.6 SD	93.4 SD	

Table 8. Lot 1 Diode Electrical Characterization (Cont)

Wafer 3	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die	01	09	100V	1.52V	6.10V	10.8V	
10^{16}	02	04	160	1.38	4.8	10.8	
cm^{-3}	07	04	170	2.40	1.2	51.0	
64	11	02	160	3.05	14.4	41.0	
		05	152	2.77	13.6	41.5	
		08	170	2.80	13.0	37.0	
44	01	09	200	1.24	4.3	9.0	
	02	04	200	1.00	6.1	17.0	
	07	04	250	4.05	40.0	80.0	
	11	02	210	3.20	16.0	40.0	
		05	190	2.00	14.0	46.0	
		08	190	2.33	10.2	25.0	
15	01	09	200	1.42	5.4	16.2	
	02	04	235	2.05	9.4	30.0	
	07	04	270	3.55	34.0	73.0	
	11	02	250	5.15	41.0	72.0	
		05	275	--	--	--	
		08	250	4.05	34.0	83.0	
41	01	09	205	1.41	5.4	14.0	
	02	04	245	2.15	9.0	30.0	
	07	04	255	3.40	26.0	70.0	
	11	02	200	4.15	25.5	70.0	
		05	195	3.17	17.4	70.0	
		08	220	3.15	16.0	64.0	
32	01	09	200	1.00	9.0	34.0	
	02	04	245	3.35	--	44.0	
	07	04	205	--	--	85.0 BD	
	11	02	270	--	--	NM	
		05	200	--	--	NM	
		08	275	--	--	NM	
Avg. of	01	09	193	1.40	6.0	10.0	
5 Die	02	04	217	2.11	7.5	20.5	
	07	04	244	3.37	27.5	70.0	
	11	02	232	3.90	24.2	60.0	
		05	210	2.81	15.0	64.5	
		08	221	3.24	10.3	50.0	

Table 8. Lot 1 Diode Electrical Characterization (Cont)

Wafer 4	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die	01	03	25.8V	0.55V	0.86V	0.75V	1.82V
10^{17}	02	04	25.8	0.92	1.42	1.84	4.80
cm^{-3}	07	04	25.5	0.88	0.78	0.97	3.75
64	11	02	24.5	0.57	0.76	0.95	3.75
		05	24.4	0.57	0.76	0.94	3.70
		08	24.7	0.56	0.75	0.92	3.50
44	01	03	25.0	0.56	0.86	0.74	1.82
	02	04	24.5	0.88	1.00	1.22	3.20
	07	04	27.0	0.71	1.22	1.84	5.50
	11	02	24.8	0.56	0.76	0.94	3.88
		05	24.5	0.56	0.76	0.93	3.85
		08	24.7	0.58	0.81	1.04	3.80
15	01	03	24.5	0.56	0.87	0.75	1.96
	02	04	24.5	0.59	0.84	1.04	5.45
	07	04	24.4	0.61	0.79	0.97	3.70
	11	02	24.8	0.57	0.77	0.96	3.85
		05	25.0	0.78	1.28	1.88	6.80
		08	24.8	0.87	1.02	1.32	4.90
41	01	03	24.0	0.56	0.86	0.75	1.85
	02	04	18.0	0.78	1.08	1.26	3.80
	07	04	25.0	0.88	0.78	0.97	3.76
	11	02	24.5	0.57	0.76	0.95	3.77
		05	25.0	0.57	0.76	0.95	3.74
		08	23.5	0.57	0.75	0.92	3.55
32	01	03	25.0	0.54	0.86	0.74	1.81
	02	04	25.0	0.57	0.82	1.00	2.90
	07	04	25.6	0.58	0.78	0.96	3.85
	11	02	24.3	0.83	0.98	1.27	4.93
		05	23.5	0.82	0.96	1.24	4.80
		08	25.0	0.56	0.74	0.92	3.83
Avg. of	01	03	24.7	0.56	0.86	0.75	1.81
5 Die	02	04	21.9	0.71	1.03	1.27	3.87
	07	04	25.5	0.82	0.87	1.10	4.87
	11	02	24.5	0.56	0.81	1.01	4.00
		05	24.5	0.82	0.90	1.15	4.38
		08	24.5	0.58	0.81	1.02	3.90

Table 8. Lot 1 Diode Electrical Characterization (Cont)

Wafer 5	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die	01	09	11.6V	0.58V	0.66V	0.69V	1.26V
$5 \cdot 10^{17}$	02	04	12.3	0.59	0.77	0.89	1.74
cm^{-3}	07	04	11.8	0.62	0.71	0.77	1.58
64	11	02	11.4	0.58	0.66	0.74	1.57
		05	11.8	0.58	0.68	0.74	1.52
		08	11.6	0.59	0.68	0.74	1.48
44	01	09	11.3	0.58	0.65	0.69	1.84
	02	04	11.6	0.56	0.68	0.75	1.48
	07	04	11.7	0.61	0.70	0.76	1.58
	11	02	11.5	0.58	0.67	0.73	1.45
		05	11.8	0.58	0.69	0.77	1.60
		08	11.3	0.58	0.67	0.73	1.38
15	01	09	11.7	0.57	0.65	0.69	1.83
	02	04	11.6	0.55	0.64	0.68	1.86
	07	04	11.9	0.61	0.70	0.76	1.58
	11	02	11.5	0.57	0.67	0.73	1.46
		05	11.7	0.57	0.67	0.73	1.48
		08	11.7	0.57	0.66	0.72	1.38
41	01	09	11.7	0.58	0.65	0.69	1.85
	02	04	11.5	0.55	0.64	0.68	1.84
	07	04	11.5	0.61	0.70	0.76	1.52
	11	02	11.5	0.57	0.67	0.73	1.46
		05	11.4	0.57	0.67	0.74	1.48
		08	11.3	0.57	0.67	0.74	1.48
32	01	09	11.6	0.58	0.66	0.70	1.85
	02	04	11.9	0.58	0.65	0.69	1.84
	07	04	11.8	0.61	0.70	0.76	1.58
	11	02	11.7	0.58	0.67	0.74	1.48
		05	11.7	0.58	0.67	0.74	1.48
		08	11.6	0.58	0.67	0.73	1.46
Avg. of	01	09	11.6	0.58	0.66	0.69	1.89
5 Die	02	04	11.8	0.57	0.69	0.74	1.26
	07	04	11.7	0.61	0.70	0.76	1.52
	11	02	11.5	0.58	0.67	0.73	1.46
		05	11.7	0.58	0.67	0.74	1.51
		08	11.5	0.58	0.67	0.73	1.43

Table 9. Lot 2 Diode Electrical Characterization

Wafer 1	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 64	01	09	250 →	2.00	7.9	16.6	37 BD
	02	04	200 →	1.71	7.3	21.4	50 BD
	07	04	300 →	3.20	15.4	32.0	75 BD
	11	02	220 →	6.50	45.0	66 BD	67 BD
		05	250 →	9.50	52.5	55 BD	--
		08	240 →	6.00	42.5	65 BD	--
44	01	09	220 →	1.40	4.34	8.3	39 BD
	02	04	180 →	1.20	4.10	8.2	50 BD
	07	04	320 →	2.50	10.00	24.0	72 BD
	11	02	200 →	2.90	13.80	48.0	60 BD
		05	190 →	2.55	10.80	25.0	54 BD
		08	190 →	1.86	7.30	15.6	56 BD
15	01	09	280 →	2.70	12.2	21.0	43 BD
	02	04	250 →	1.95	9.3	36.0	60 BD
	07	04	370 →	4.70	23.3	38.0	80 BD
	11	02	280 →	6.90	56.0	66 BD	66 BD
		05	280 →	6.50	46.5	54 BD	--
		08	280 →	3.60	20.0	62.5	66 BD
41	01	09	250 →	1.28	3.50	6.10	38 BD
	02	04	220 →	1.20	3.10	5.70	50 BD
	07	04	280 →	2.10	7.50	17.00	88 BD
	11	02	220 →	2.05	7.20	16.00	60 BD
		05	250 →	2.00	10.40	27.00	58 BD
		08	--	1.80	6.90	14.60	58 BD
32	01	09	230 →	1.65	5.60	11.80	42 BD
	02	04	170 →	1.40	5.00	11.20	55 BD
	07	04	250 →	2.65	12.00	26.00	75 BD
	11	02	180 →	4.00	21.00	61.00	65 BD
		05	220 →	5.00	35.00	60 BD	--
		08	200 →	3.30	16.80	48.0	75 BD
Avg. of 5 Die	01	09	246 →	1.81	6.71	12.76	38.8 BD
	02	04	204 →	1.40	5.76	16.56	53.8 BD
	07	04	304 →	3.07	13.84	27.40	78.8 BD
	11	02	220 →	4.47	28.00	51.00	63.6 BD
		05	236 →	5.35	31.04	44.20	56.0 BD
		08	228 →	3.31	16.70	41.14	63.8 BD

Table 9. Lot 2 Diode Electrical Characterization (Cont)

Wafer 2	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 64	01	09	50.0 soft	1.90	7.60	15.0	60 BD
	02	04	100 →	1.60	5.80	10.8	50 BD
	07	04	140 →	4.80	23.0	42.5	100 BD
	11	02	88.0 →	6.00	27.2	50.5	87 BD
		05	100 →	5.50	24.6	46.5	88 BD
		08	90.0 →	4.80	21.5	42.0	91 BD
44	01	09	130.0 →	2.00	7.90	8.60	50 BD
	02	04	94.0 →	1.60	6.00	11.8	60 BD
	07	04	180.0 →	4.00	19.2	38.0	95 BD
	11	02	120.0 →	5.05	24.0	49.0	70 BD
		05	140.0 →	5.50	26.4	53.0	70 BD
		08	140.0 →	4.80	23.0	48.0	70 BD
15	01	09	120.0 →	1.14	3.40	6.20	45 BD
	02	04	80.0 →	0.97	2.66	4.70	50 BD
	07	04	140.0 →	1.88	7.00	14.2	82 BD
	11	02	100.0 →	2.75	9.00	18.0	62 BD
		05	100.0 →	2.80	9.10	18.2	62 BD
		08	90.0 →	2.50	7.70	15.4	64 BD
41	01	09	120.0 →	1.48	5.20	10.7	47 BD
	02	04	100.0 →	1.26	4.20	8.20	50 BD
	07	04	160.0 →	3.05	14.4	32.7	84 BD
	11	02	120.0 →	3.64	17.4	38.6	67 BD
		05	130.0 →	4.10	20.0	42.8	68 BD
		08	130.0 →	3.70	17.7	38.0	65 BD
32	01	09	100.0 →	1.75	6.35	12.6	56 BD
	02	04	80.0 →	1.30	4.30	8.00	60 BD
	07	04	150.0 →	3.50	16.0	35.0	82 BD
	11	02	100.0 →	4.00	18.0	35.0	68 BD
		05	110.0 →	4.20	19.0	37.6	70 BD
		08	106.0 →	3.70	16.2	32.5	72 BD
Avg. of 5 Die	01	09	104.0 →	1.65	6.08	10.6	52 BD
	02	04	96.8 →	1.35	4.58	8.70	64 BD
	07	04	154.0 →	3.45	16.0	32.5	89 BD
	11	02	105.6 →	4.29	19.1	38.2	71 BD
		05	116.6 →	4.42	20.0	39.5	70 BD
		08	116.0 →	3.90	17.2	35.2	72 BD

Table 9. Lot 2 Diode Electrical Characterization (Cont)

Wafer 4	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 64	01	09	25.0	0.57	0.74	0.88	3.10
	02	04	25.0	0.56	0.72	0.85	2.85
	07	04	26.0	0.64	0.97	1.31	7.10
	11	02	26.0	0.61	0.93	1.28	7.00
		05	25.0	0.61	0.96	1.32	7.10
		08	16.8 soft	0.61	0.92	1.24	6.50
44	01	09	24.0	0.58	0.73	0.87	2.90
	02	04	23.0 soft	0.56	0.71	0.83	2.65
	07	04	25.0	0.64	0.95	1.28	6.80
	11	02	24.0	0.61	0.90	1.23	6.25
		05	23.0	0.60	0.89	1.19	6.10
		08	24.0	0.60	0.87	1.15	5.70
15	01	09	23.0	0.60	0.77	0.92	3.00
	02	04	23.0 soft	0.62	0.87	1.04	2.90
	07	04	24.0	0.66	0.98	1.32	6.60
	11	02	24.0	0.65	1.04	1.40	6.50
		05	23.0	0.63	0.94	1.26	6.40
		08	24.0 soft	0.61	0.89	1.18	5.80
41	01	09	24.0	0.58	0.74	0.88	3.00
	02	04	24.0	0.57	0.72	0.84	2.66
	07	04	25.0	0.65	0.97	1.31	6.80
	11	02	24.0	0.61	0.89	1.18	6.00
		05	23.0	0.61	0.89	1.18	5.90
		08	24.0	0.61	0.87	1.14	5.60
32	01	09	23.0 soft	0.59	0.75	0.91	3.25
	02	04	24.0 soft	0.57	0.73	0.88	2.70
	07	04	25.0	0.64	0.96	1.29	6.60
	11	02	25.0	0.61	0.91	1.22	6.40
		05	24.0	0.62	0.91	1.22	6.30
		08	25.0	0.61	0.89	1.18	5.90
Avg. of 5 Die	01	09	24.0	0.58	0.75	0.89	3.05
	02	04	24.0	0.58	0.75	0.90	2.75
	07	04	25.0	0.65	0.97	1.30	6.78
	11	02	25.0	0.62	0.93	1.26	6.43
		05	24.0	0.61	0.92	1.23	6.36
		08	23.0	0.61	0.89	1.18	5.90

Table 9. Lot 2 Diode Electrical Characterization (Cont)

Wafer 5	Structure	Diode	BV_D at 10 μA	V_f at I_f = 10 μA	V_f at I_f = 50 μA	V_f at I_f = 100 μA	V_f at I_f = 1 mA
Die 64	01	09	12.00	0.57	0.65	0.70	1.16
	02	04	12.00	0.55	0.64	0.68	1.08
	07	04	12.00	0.60	0.70	0.77	1.88
	11	02	11.80	0.57	0.67	0.75	1.84
		05	11.80	0.57	0.67	0.75	1.62
		08	12.00	0.57	0.67	0.74	1.58
44	01	09	11.50	0.57	0.65	0.69	1.08
	02	04	11.50 soft	0.35	0.64	0.68	1.06
	07	04	11.60	0.60	0.70	0.77	1.80
	11	02	11.30 soft	0.57	0.67	0.74	1.53
		05	11.20 soft	0.57	0.67	0.74	1.52
		08	11.20	0.57	0.67	0.73	1.48
15	01	09	11.80	0.58	0.66	0.70	1.15
	02	04	11.80	0.56	0.64	0.69	1.11
	07	04	11.60	0.61	0.71	0.78	1.68
	11	02	11.90	0.58	0.68	0.76	1.67
		05	11.80	0.58	0.68	0.75	1.66
		08	11.80	0.58	0.68	0.75	1.62
41	01	09	5.10 soft	0.56	0.64	0.69	1.10
	02	04	11.80	0.54	0.64	0.69	1.22
	07	04	12.00	0.60	0.70	0.78	1.78
	11	02	11.90	0.58	0.69	0.79	1.88
		05	7.90 soft	0.56	0.66	0.74	1.60
		08	12.00	0.56	0.66	0.74	1.57
32	01	09	11.80 soft	0.58	0.66	0.71	1.16
	02	04	11.70	0.56	0.65	0.70	1.12
	07	04	11.40 soft	0.61	0.71	0.78	1.73
	11	02	11.80	0.58	0.68	0.75	1.64
		05	11.80	0.59	0.69	0.78	1.80
		08	11.80	0.59	0.68	0.75	1.58
Avg. of 5 Die	01	09	10.40	0.57	0.65	0.70	1.13
	02	04	11.72	0.55	0.64	0.69	1.12
	07	04	11.72	0.60	0.70	0.78	1.69
	11	02	11.74	0.58	0.68	0.76	1.66
		05	10.90	0.57	0.67	0.75	1.64
		08	11.72	0.57	0.67	0.74	1.57

Table 10. Lot 1 Diode Data Summary

$N_D\left(\frac{atoms}{cm^3}\right)$		1	2	3	4	5
Diode	Parameter	10^{14}	10^{15}	10^{16}	10^{17}	$5x10^{17}$
01, 09	BVD at 10 μA	182	232	193	24.7	11.6
	V_f at 10 μA	8.2	25.7	1.48	0.55	0.58
	V_f at 50	22.6	61.6	6.9	0.66	0.65
	V_f at 100	27.6	65.5 BD	18.6	0.75	0.89
	V_f at 1 mA	35.5	72.0 BD	--	1.81	1.09
02, 04	BVD at 10 μA	199	268	217	21.9	11.8
	V_f at 10 μA	8.3	30.7	2.11	0.71	0.57
	V_f at 50	19.7	67.7	7.5	1.03	0.68
	V_f at 100	24.2	74.9	26.5	1.27	0.74
	V_f at 1 mA	34.1	82.1 BD	--	3.87	1.26
07, 04	BVD at 10 μA	184	205	244	25.5	11.7
	V_f at 10 μA	16.3	49.9	3.37	0.62	0.61
	V_f at 50	46.6	95.2	27.5	0.87	0.70
	V_f at 100	55.1	109.3	70.8	1.10	0.76
	V_f at 1 mA	71.1	136.5 BD	--	4.87	1.52
11, 02	BVD at 10 μA	196	298	232	24.5	11.5
	V_f at 10 μA	19.2	88.1	3.89	0.58	0.58
	V_f at 50	34.5	91.4 BD	24.2	0.81	0.67
	V_f at 100	40.4	92.8 BD	88.8	1.01	0.73
	V_f at 1 mA	77.6	--	--	4.00	1.48
11, 05	BVD at 10 μA	201	318	218	24.5	11.7
	V_f at 10 μA	21.2	36.8	2.91	0.62	0.58
	V_f at 50	38.6	99.4 BD	15.8	0.90	0.67
	V_f at 100	45.6	100.8 BD	54.5	1.15	0.74
	V_f at 1 mA	83.1	--	--	4.38	1.51
11, 08	BVD at 10 μA	202	323	221	24.5	11.5
	V_f at 10 μA	19.6	86.3	3.24	0.58	0.58
	V_f at 50	37.3	93.6 BD	16.3	0.81	0.67
	V_f at 100	43.3	93.4 BD	58.8	1.02	0.73
	V_f at 1 mA	79.8	--	--	3.90	1.43

Table 11. Lot 2 Diode Data Summary

$X_E = 30\ \mu M$

$N_D \left(\frac{atoms}{cm^3}\right)$		1	2	3	4	5
Diode	Parameter	10^{14}	10^{15}	10^{16}	10^{17}	5×10^{17}
01, 09	BVD at 10 μA	240 →	184.0 →		24.0	10.40
	V_f at 10 μA	1.81	1.85		0.58	0.57
	V_f at 50	6.71	6.00		0.75	0.85
	V_f at 100	12.76	10.5		0.00	0.70
	V_f at 1 mA	30.0 B_D	52.0 B_D		3.05	1.13
02, 04	BVD at 10 μA	204 →	90.0 →		24.0	11.72
	V_f at 10 μA	1.40	1.35		0.58	0.55
	V_f at 50	5.76	4.50		0.75	0.04
	V_f at 100	10.50	8.70		0.90	0.00
	V_f at 1 mA	53.0 B_D	54.0 B_D		2.75	1.12
07, 04	BVD at 10 μA	304 →	154.0 →		25.0	11.72
	V_f at 10 μA	3.07	3.45		0.05	0.00
	V_f at 50	13.04	10.0		0.07	0.70
	V_f at 100	27.40	32.5		1.30	0.70
	V_f at 1 mA	70.0 B_D	00.0 B_D		0.70	1.00
11, 02	BVD at 10 μA	220 →	105.5 →		25.0	11.74
	V_f at 10 μA	4.47	4.20		0.02	0.50
	V_f at 50	20.00	10.1		0.03	0.00
	V_f at 100	51.00	30.2		1.20	0.70
	V_f at 1 mA	03.0 B_D	71.0 B_D		0.03	1.00
11, 05	BVD at 10 μA	230 →	110.0 →		24.0	10.00
	V_f at 10 μA	5.35	4.42		0.01	0.57
	V_f at 50	31.04	20.2		0.02	0.07
	V_f at 100	44.20	30.5		1.23	0.75
	V_f at 1 mA	50.0 B_D	70.0 B_D		0.30	1.04
11, 00	BVD at 10 μA	220 →	110.0 →		23.0	11.72
	V_f at 10 μA	3.31	3.00		0.01	0.57
	V_f at 50	10.70	17.2		0.00	0.07
	V_f at 100	41.14	35.2		1.10	0.74
	V_f at 1 mA	03.0 B_D	72.0 B_D		0.00	1.57

III. CONCLUSIONS

The objective of this contractual effort has been met. That is, a complement of SOS p-n diodes with a full range of process parameter variations and physical design variations has been provided to aid in isolating the precise mechanisms of second breakdown. All design goals of the special advanced structures were accomplished.

IV. RECOMMENDATIONS

It is anticipated that new device design requirements will arise as Auburn University progresses through their second breakdown tests. These tests will also produce a large set of devices which have been stressed to catostrophic failure. It will be necessary to determine precisely how the failures occurred. For example, was the metal spike responsible for initiating the melt path? It is therefore recommended that a failure analysis effort be incorporated into the existing program to determine, in detail, the actual causes of failure. Secondly, it is recommended that additional wafer lots, reflecting new design, test and analysis results be planned for the program.

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APPENDIX

STROBOSCOPIC EXPERIMENTAL ARRANGEMENT AS DESCRIBED IN REFERENCE 7

STROBOSCOPIC ARRANGEMENT

An inverted metallurgical microscope (Unitron) was used for observing the light transmitted by the silicon-on-sapphire diodes (see Figure A-1). The inverted configuration allows current probes and microscope objectives to be positioned independently and without interference with each other. This is necessary both for convenience and because high power objectives must be within 0.3 mm of the surface observation. An eight-inch square of steel sheet was screwed to the regular microscope stage, increasing its area to accommodate movable current probes. The probes (Wentworth Laboratories Model PR-0160) were held in a fixture with a permanent magnet base. No special holder was required for the devices because the magnetically secured probes firmly constrained the test wafer. The stage could be translated across the microscope objective to view the diode to be tested. A low-power, long working distance stereomicroscope was located above the stage and used to position the probes.

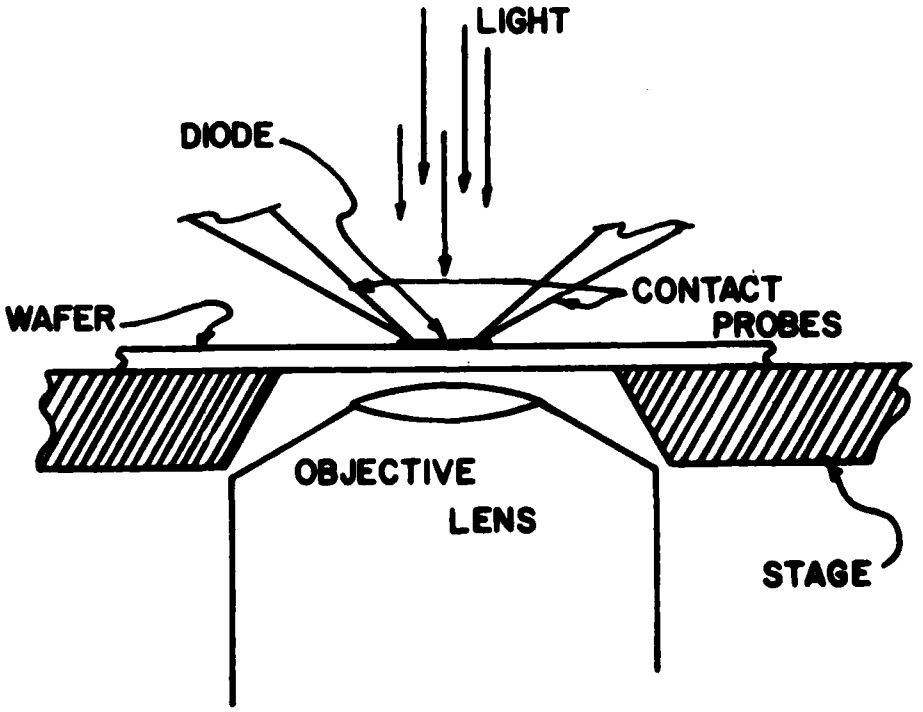

Figure A-1. A Silicon-on-Sapphire Diode in Position for Observation of Second Breakdown Phenomena. The wafer, probes and stage are moved as a unit to select the area of observation. (Reference 7)

The diodes were illuminated from above by a pulsed arc source focused by a 50 mm camera lens. A Xenon Corporation open electric arc (Nanolamp) with power supply (Model 437 Nanopulser) and external trigger provided a broad-band output with a peak intensity of 50,000 watts, pulse duration of 10 nsec, pulse repetition rate of 0 to 100 per second, and a jitter relative to the trigger signal of about 1 μsec. This light source has its spectral output in the sensitive range of conventional photographic emulsions. Its brightness in the visible range is sufficient that no image intensification is required for direct microscopic observations. Its broad band precludes interpretive problems due to interference effects associated with internal reflections in the silicon layer and the sapphire substrate. Thus, it is a far superior source for stroboscopic studies than Sunshine's AlGaAs laser (10 nsec pulses, 7100Å, liquid-nitrogen cooled), which required image intensification, could not be used with photographic materials because of the low sensitivity of photographic emulsions to the far red, and the interpretive problems associated with interference effects.

Electrical excitation of the diodes was done with constant current pulses, variable in amplitude up to 750 mA, into a 100 ohm load. This capability proved to be more than adequate for the purposes of this work. Most testing was done with pulses of 100 μsec duration and at a repetition rate of 0 - 100 pps. When desired, the circuit could be operated in a single-pulse mode.

A block diagram of the complete stroboscopic system is shown in Figure A-2. A Hewlett-Packard Model 214A pulse generator provides a variable width rectangular voltage pulse and a trigger pulse whose position in time relative to the leading edge of the rectangular voltage pulse can be continuously delayed or advanced up to 10 msec. The main pulse is used to drive the constant current amplifier, which, in turn, applies a current pulse to the device under investigation. The trigger output from the HP 214A determines the time at which the strobe light is excited. However, the trigger pulse from the HP 214A was inadequate to drive the Nanopulse control, so a GR Model 1217B pulse generator is used to obtain an effective trigger pulse. The waveforms of the voltage across the test device and the current through it were displayed on a dual-trace oscilloscope (Tektronix Model 551).

Finally, the actual firing time of the light source with respect to the initial rise of the current pulse was established using a CdS photocell mounted beside the light source to detect the flash. The output signal from the photocell goes through an RC pulse shaping network which controls the beam intensity of the oscilloscope. The display on the CRO thus shows the voltage and current waveforms with a bright spot marker on both traces indicating the position of the light flash relative to the electrical pulse.

At very high current levels, significant damage occurs on every pulse, so it is desirable to be able to employ single pulses. Such a capability also assures that no information is obscured by operation in the stroboscopic mode, as might occur if the locus of a current channel shifted from pulse to pulse. By focusing the light from the pulsed source to a spot slightly larger than the specimen and using Kodak Tri-X or Polaroid 3000 ASA film, single pulse events could be photographed with a 5X microscope objective. The results of this type of single event photography were useful in establishing the repeatability of the stroboscopic mode. In most cases

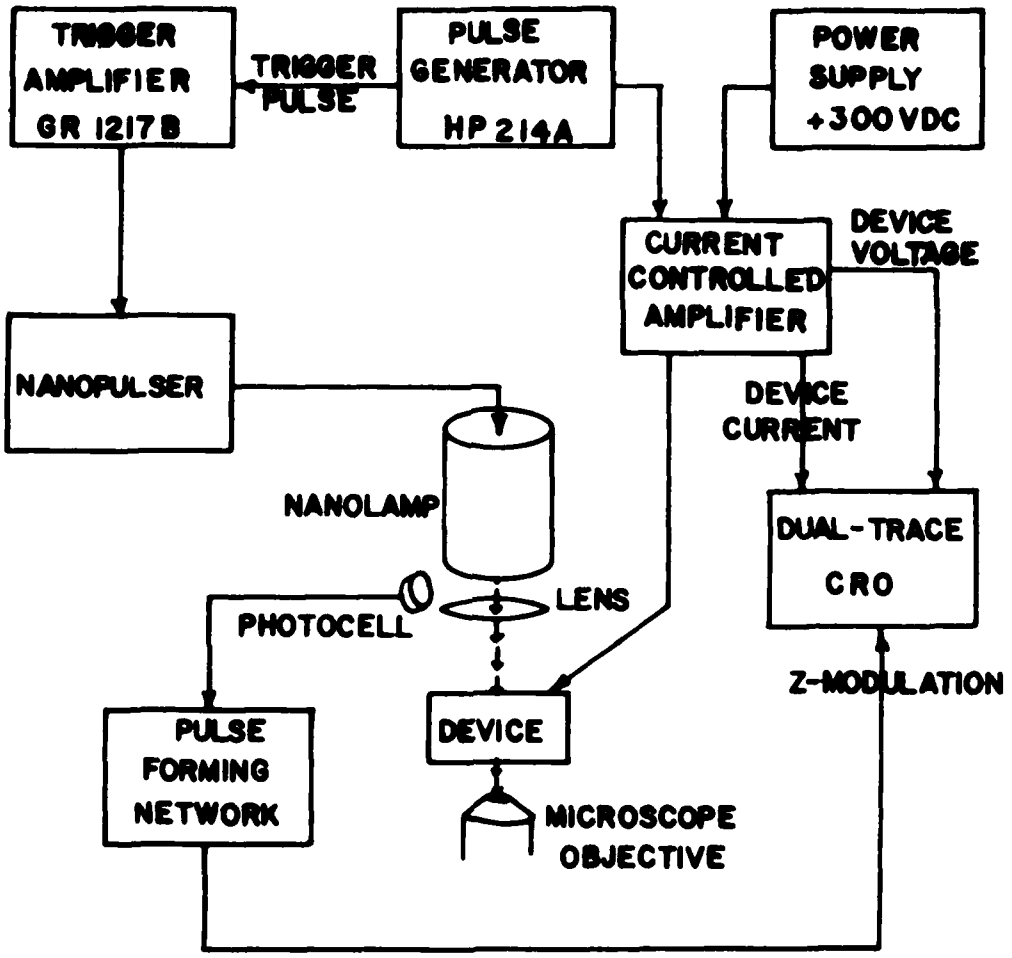

Figure A-2. Block Diagram of the Apparatus for Stroboscopic Observations of Optical Transmission Patterns of Silicon-on-Sapphire Devices under Electrical Stress (Reference D1)

not involving damage, the system was repetitively pulsed because visual and photographic observations could be more easily made with repetitive than with single pulses.

Diodes emit light during avalanche, filamentation, and second breakdown. The photographic arrangement of the stroboscopic setup can be used to record this emission. The integrated intensity of each pulse is obtained, since no shutter was available to stroboscopically examine the emitted light Normally it is necessary to integrate over a number of pulses to obtain good photographs.

By placing a photomultiplier in the film plane of the camera with a small aperture over the cathode window, it was possible to use the calibrated temperature dependence of the optical transmittance of the silicon to measure temperatures within the device. This arrangement has the potential of making temperature measurements from room temperature up to about 700C, with a time resolution of 10 nsec, and a spatial resolution of 10 microns.

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ATTN: NTYC, Mullis
ATTN: NTYC, R. Maier
ATTN: NTYC, M. Schneider
5 cy ATTN: NTYC

Air Force Wright Aeronautical Lab
ATTN: POD, P. Stover
ATTN: POE-2, J. Wise

DEPARTMENT OF THE AIR FORCE (Continued)

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ATTN: DH, J. McKenzie
ATTN: DHE-2
ATTN: DHE

Air Logistics Command
Department of the Air Force
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Air University Library
Department of the Air Force
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Assistant Chief of Staff
Studies & Analyses
Department of the Air Force
ATTN: AF/SAMI

Ballistic Missile Office
Air Force Systems Command
ATTN: ENSN, H. Ward

Ballistic Missile Office
Air Force Systems Command
ATTN: Hq Space Div/RSMG, E. Collier
ATTN: ENSN
ATTN: ENSN, J. Tucker
ATTN: ENBE
ATTN: ENMG
ATTN: SYDT

Electronic Systems Division
Department of the Air Force
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Foreign Technology Division
Air Force Systems Command
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ATTN: TQTD, B. Ballard

Headquarters Space Division
Air Force Systems Command
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ATTN: AQT, W. Blakney

Headquarters Space Division
Air Force Systems Command
ATTN: SKF, P. Stadler

Headquarters Space Division
Air Force Systems Command
ATTN: SZJ, R. Davis

Headquarters Space Division
Air Force Systems Command
ATTN: YLS

Rome Air Development Center
Air Force Systems Command
ATTN: RBRAC, I. Krulac
ATTN: RBRP, C. Lane

Strategic Air Command
Department of the Air Force
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ATTN: XPFS, M. Carra

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ATTN: ESR, B. Buchanan
ATTN: ESR, W. Shedd
ATTN: ESE, A. Kahan

3416th Technical Training Squadron (ATC)
Air Training Command
Department of the Air Force
ATTN: TTV

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Department of Energy
Albuquerque Operations Office
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ATTN: WSSB, R. Shay

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ATTN: OSWR/NED

Department of Commerce
National Bureau of Standards
ATTN: Sec Ofc for J. French
ATTN: Sec Ofc for J. Humphreys
ATTN: Sec Ofc for K. Galloway

Department of Transportation
Federal Aviation Administration
ATTN: ARD-350

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Goddard Space Flight Center
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NASA
George C. Marshall Space Flight Center
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ATTN: L. Haniter
ATTN: EG02

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ATTN: L-153, D. Meeker

Los Alamos National Laboratory
ATTN: J. Freed

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ATTN: H. Sisler

University of Oklahoma
ATTN: R. Wood

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ATTN: D. Fresh
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ATTN: R. Crolius
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ATTN: J. Reinheimer

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Avco Research & Systems Group
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ATTN: D. Hamman

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ATTN: R. Pease
ATTN: Marketing
ATTN: D. Alexander

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ATTN: Document Control

Bendix Corp
ATTN: M. Frank

Bendix Corp
ATTN: E. Meeder

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ATTN: H. Wicklein
ATTN: D. Egelkrout
ATTN: 8K-38
ATTN: R. Caldwell

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ATTN: I. Arimura

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ATTN: C. Stump

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University of Denver
ATTN: Sec Officer for F. Venditti

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Ex-Cal, Inc
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Exp & Math Physics Consultants
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ATTN: K. Attinger
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General Dynamics Corp
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ATTN: R. Fields

General Electric Co
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ATTN: R. Casey
ATTN: L. Sivo
ATTN: Technical Info Ctr for L. Chasen
ATTN: J. Andrews
ATTN: J. Peden

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ATTN: J. Palchefsky, Jr
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George C. Messenger
Consulting Engineer
ATTN: G. Messenger

Georgia Institute of Technology
ATTN: R. Curry

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Goodyear Aerospace Corp
ATTN: Security Control Station

Grumman Aerospace Corp
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ATTN: J. Cornell
ATTN: C. Anderson
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ATTN: MS 725-5

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ATTN: D. Binder
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IBM Corp
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ATTN: Electromagnetic Compatability
ATTN: T. Martin
ATTN: H. Mathers

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IIT Research Institute
ATTN: I. Mindel

Institute for Defense Analyses
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International Business Machine Corp
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International Tel & Telegraph Corp
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ATTN: A. Richardson

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Ion Physics Corp
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ATTN: W. Rich
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ATTN: W. Ware

Kaman Tempo
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ATTN: M. Espig
ATTN: W. McNamara
ATTN: DASIAC

Kaman Tempo
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ATTN: J. Crowley

Lockheed Missiles & Space Co, Inc
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ATTN: P. Bene
ATTN: D. Phillips/DPT 62-46

M.I.T. Lincoln Lab
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Martin Marietta Corp
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ATTN: TIC/MP-30

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Motorola, Inc
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Northrop Corp
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ATTN: D. Strobel
ATTN: Sec Ofc for T. Jackson

Pacific-Sierra Research Corp
ATTN: H. Brode

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ATTN: P. Haas

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ATTN: J. Ciccio

Raytheon Co
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ATTN: H. Flescher

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ATTN: G. Brucker

RCA Corp
ATTN: Office N103
ATTN: D. O'Connor
ATTN: L. Minich

RCA Corp
ATTN: R. Killion

RCA Corp
ATTN: W. Allen

Rensselaer Polytechnic Institute
ATTN: R. Gutmann

Research Triangle Institute
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Rockwell International Corp
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ATTN: K. Hull
ATTN: V. Michel
ATTN: J. Brandford
ATTN: V. Strahan
ATTN: N. Rudie
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Rockwell International Corp
ATTN: TIC D/41-092 AJ01

Rockwell International Corp
ATTN: T. Yates
ATTN: TIC BA08

Rockwell International Corp
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ATTN: A. Langenfeld

Sanders Associates, Inc
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ATTN: J. Naber

Science Applications, Inc
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Science Applications, Inc
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Science Applications, Inc
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Singer Co
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Sperry Rand Corp
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ATTN: R. Viola
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ATTN: F. Scaravaglione

Sperry Rand Corp
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Sperry Univac
ATTN: J. Inda

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ATTN: P. Dolan
ATTN: B. Gasten
ATTN: A. Whitson

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ATTN: Research Department

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ATTN: L. Blaisdell
ATTN: L. Pauples

Sylvania Systems Group
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ATTN: H & V Group
ATTN: J. Waldron
ATTN: P. Fredrickson

Systron-Donner Corp
ATTN: J. Indelicato

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Tetra Tech, Inc
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ATTN: A. Peletier
ATTN: R. Stehlin
ATTN: D. Manus

Texas Instruments, Inc
ATTN: F. Poblenz

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ATTN: Vulnerability & Hardness Laboratory
ATTN: W. Rowan
ATTN: P. Guilfoyle
ATTN: A. Witteles
ATTN: Technical Information Center
ATTN: A. Narevsky
ATTN: H. Holloway
2 cy ATTN: R. Plebuch
2 cy ATTN: O. Adams

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

TRW Defense & Space Sys Group
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ATTN: R. Kitter
ATTN: W. Willis, M/S RI/2078
ATTN: F. Fay

TRW Systems and Energy
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ATTN: B. Gililland
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ATTN: R. Tomme
ATTN: Technical Data Center

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ATTN: H. Kalapaca
ATTN: MS 3330

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